Synchronous 4-Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

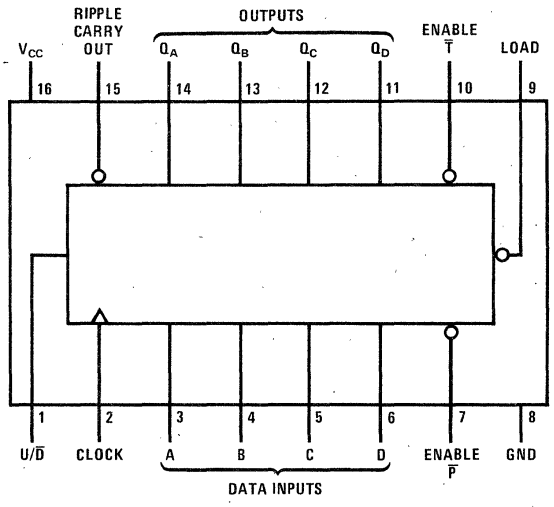
The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Fully independent clock circuit

Connection Diagram



54LS168/74LS168(J), (N), (W);
54LS169/74LS169(J), (N), (W)

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS			DM54LS/74LS168, LS169 MIN	TYP(1)	MAX	UNITS
V_{IH}	High Level Input Voltage					2			V
V_{IL}	Low Level Input Voltage				DM54			0.7	V
					DM74			0.8	
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = −18 mA					−1.5	V
I_{OH}	High Level Output Current							−400	μA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max, I_{OH} = −400μA		DM54	2.5	3.4		V
					DM74	2.7	3.4		
I_{OL}	Low Level Output Current				DM54			4	mA
					DM74			8	
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 4 mA			0.25	0.4	V
				I_{OL} = 8 mA,	DM74		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = Max, V_I = 7V					0.1	mA
		Clock, $\overline{T}$						0.2	
		Load						0.3	
I_{IH}	High Level Input Current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = Max, V_I = 2.7V					20	μA
		Clock, $\overline{T}$						40	
		Load						60	
I_{IL}	Low Level Input Current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = Max, V_I = 0.4V					−0.4	mA
		$\overline{T}$						−0.8	
		Load , Clock						−1.2	
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)			−30		−130	mA
I_{CC}	Supply Current		V_{CC} = Max(3)				20	34	mA

Notes (1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

(3) I_{CC} is measured after applying a momentary 4.5V, then ground, to the clock input with all other inputs grounded and the outputs open.

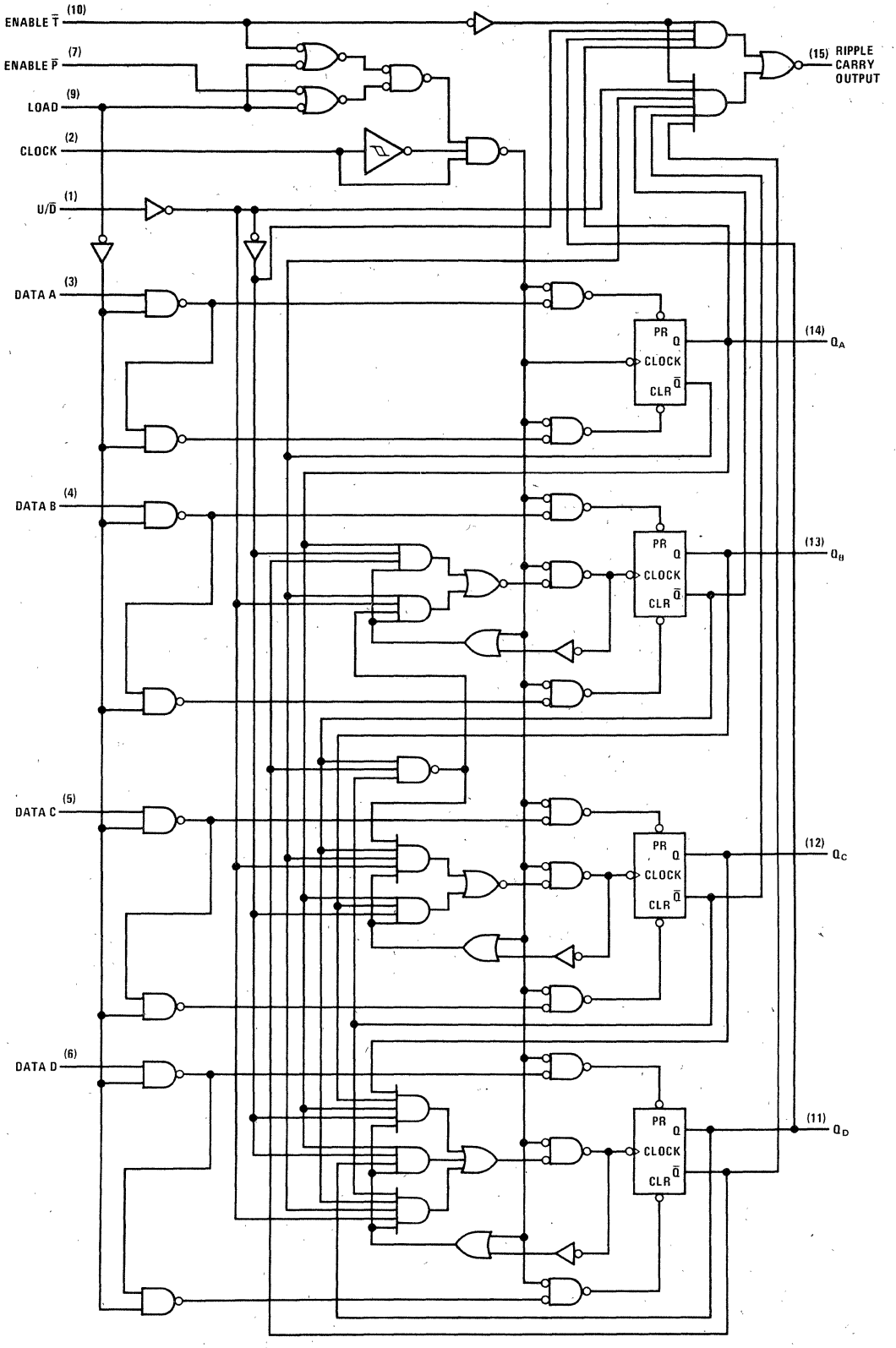
Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER			FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54LS/74LS168, LS169 MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency				C_L = 15 pF, R_L = 2 kΩ,	25	32		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Ripple Carry			23	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						23	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Clock	Any Q			13	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						15	23	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Enable $\overline{T}$	Ripple Carry			10	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						16	23	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		Up/Down (4)	Ripple Carry			17	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output						19	29	ns
$t_{W(CLOCK)}$	Width of Clock Pulse (High or Low)					25			ns
t_{SETUP}	Setup Time	Data Inputs A, B, C, D				20			ns
		Enable $\overline{P}$ or $\overline{T}$				25			
		Load				25			
		Up/Down				30			
t_{HOLD}	Hold Time	Data Inputs A, B, C, D				0			ns
		Enable $\overline{P}$ or $\overline{T}$				0			
		Load, Up/Down				0			

Notes (4) Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for LS168 or 15 for LS169), the ripple carry output will be out of phase.

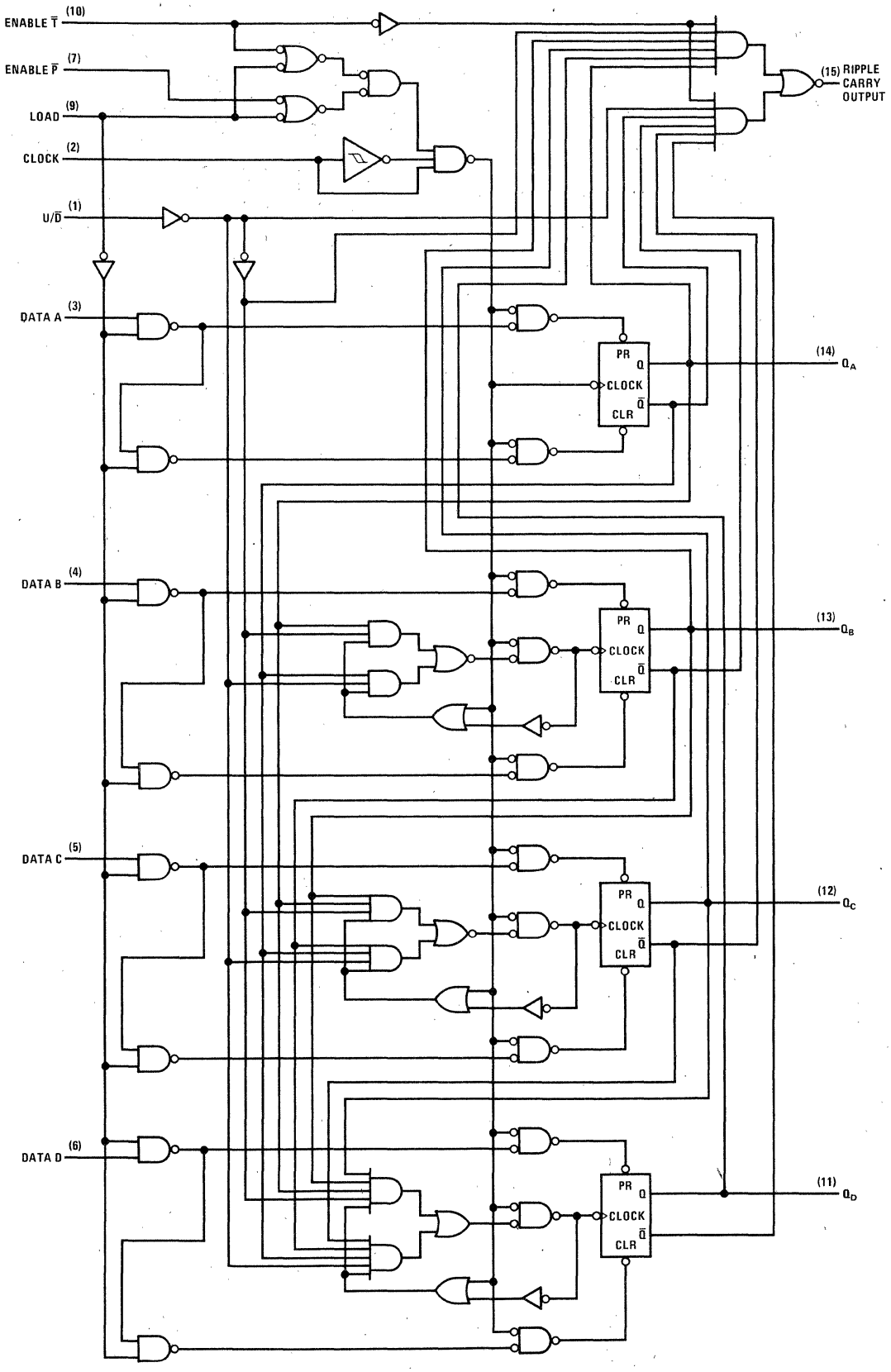
Logic Diagrams

LS168 DECADE COUNTERS



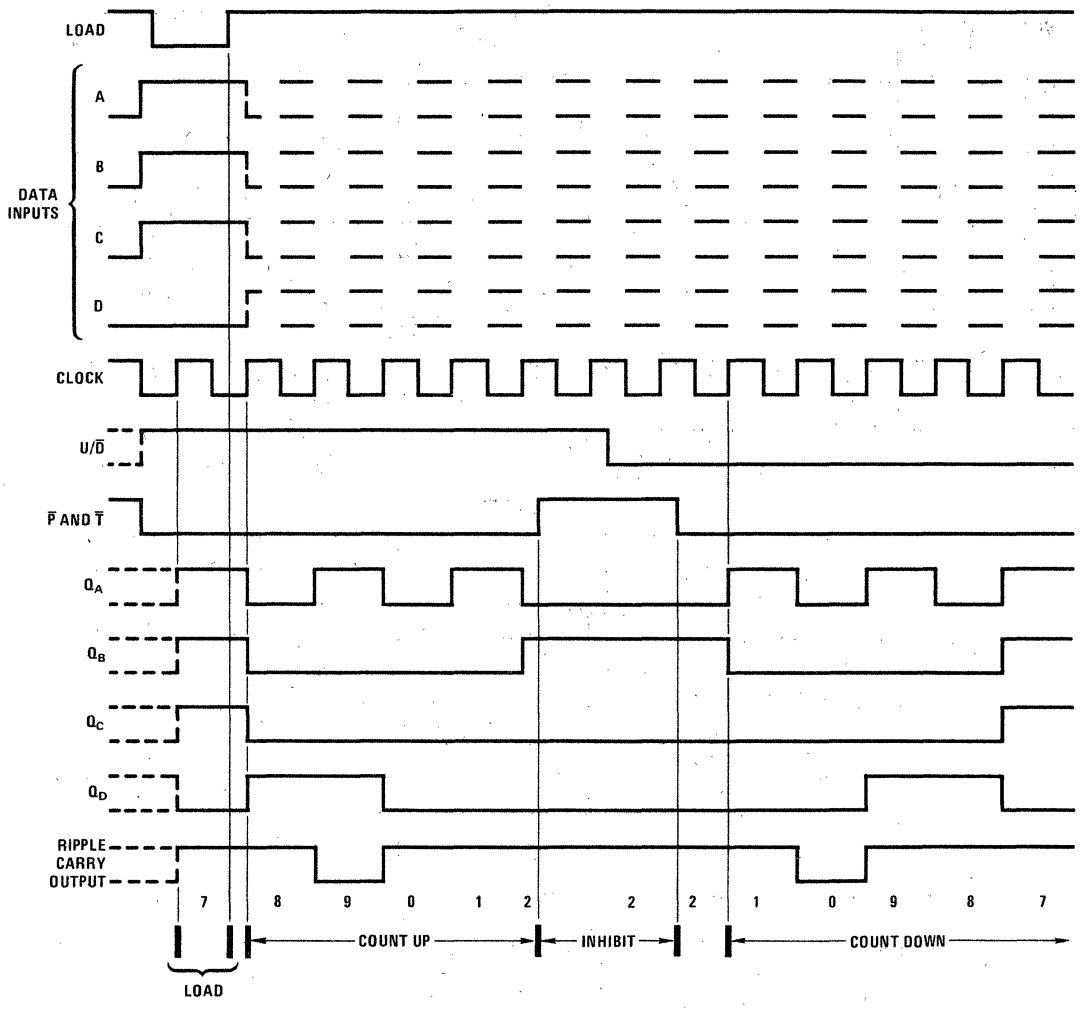
Logic Diagrams (Continued)

LS169 BINARY COUNTERS



Timing Diagrams

LS168 DECADE COUNTERS
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

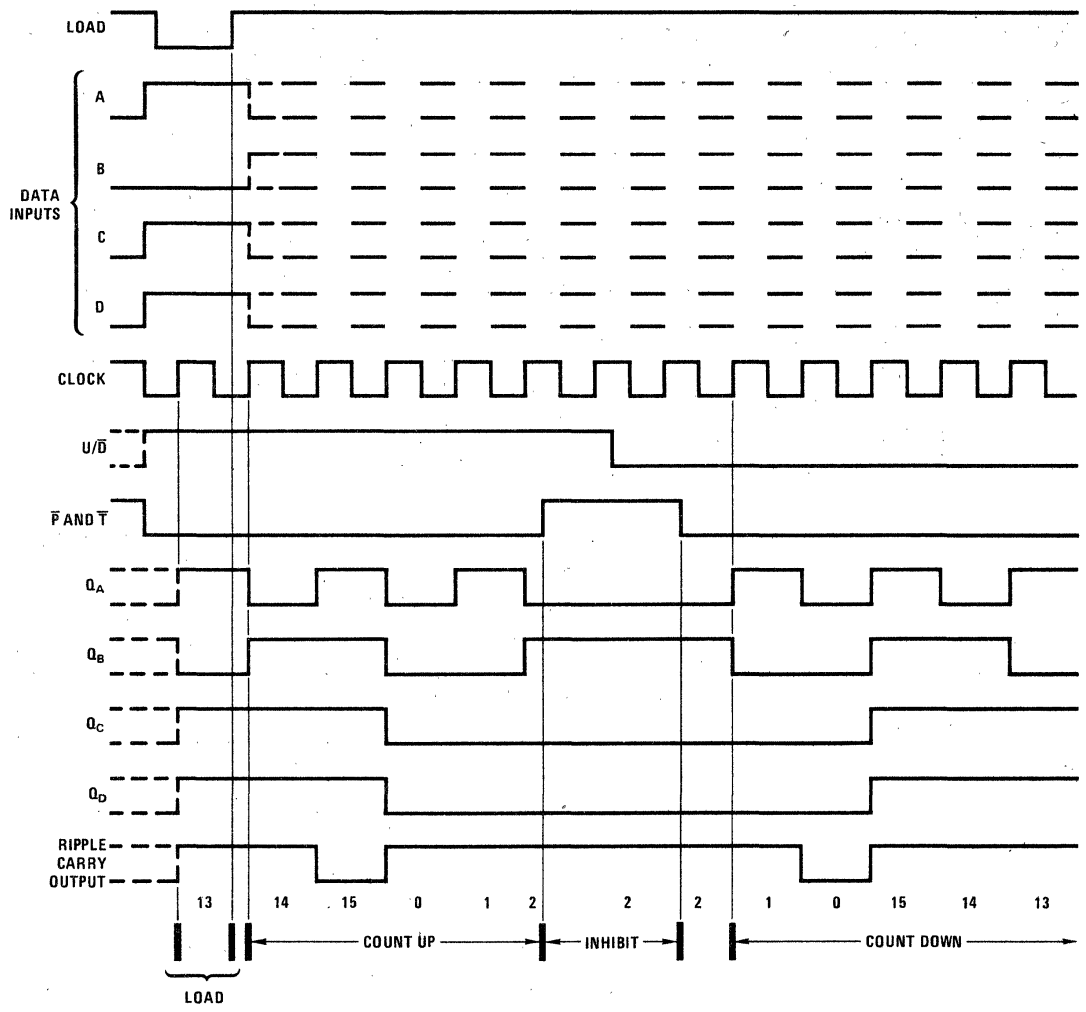


Sequence:

(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight and seven

Timing Diagrams (Continued)

LS169 BINARY COUNTERS
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES



Sequence:

(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen and thirteen