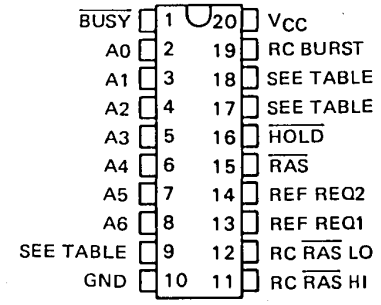
TYPES SN74LS600A THRU SN74LS603A
MEMORY REFRESH CONTROLLERS

D2547, JANUARY 1981—REVISED JUNE 1983

- Controls Refresh Cycle of 4K, 16K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- Choice of Transparent, Cycle Steal, or Burst Refresh Modes
- 3-State Outputs Drive Bus Lines Directly
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS' . . . J PACKAGE
SN74LS' . . . DW, J OR N PACKAGE
(TOP VIEW)



FOR CHIP CARRIER INFORMATION
CONTACT THE FACTORY

SELECTION TABLE

DEVICE	REFRESH MODES	MEMORY SIZE	PIN ASSIGNMENTS		
			PIN 9	PIN 17	PIN 18
'LS600A	Transparent, Burst	4K or 16K	4K/$\overline{16K}$	LATCHED RCO	RESET LATCHED RCO
'LS601A	Transparent, Burst	64K	A7	LATCHED RCO	RESET LATCHED RCO
'LS602A	Cycle Steal, Burst	4K or 16K	4K/$\overline{16K}$	$\overline{READY}$	RC CYCLE STEAL
'LS603A	Cycle Steal, Burst	64K	A7	$\overline{READY}$	RC CYCLE STEAL

description

The 'LS600A thru 'LS603A memory refresh controllers contain one 8-bit synchronous counter, nine 3-state buffer drivers, four RC-controlled multivibrators, and other control circuitry on a single monolithic chip. These devices are designed to provide RAS-only refresh on 4K, 16K, and 64K dynamic RAMs. The 'LS600A and 'LS601A provide transparent refresh while the 'LS602A and 'LS603A provide cycle-steal refresh. In addition, a burst-mode timer is provided to warn the CPU that the maximum allowable refresh time is about to be violated.

operating modes

In the transparent refresh mode ('LS600A or 'LS601A), row-refresh cycles occur only during inactive CPU-memory times. In most cases the entire memory refresh sequence can be completed "transparently" without interrupting CPU operations. During idle CPU-memory periods, the REF REQ pins should be taken high so as many rows as possible can be refreshed. A low from $\overline{BUSY}$ will signal the CPU to wait until the end of that current row refresh before reinstating operations. If all row addresses have been refreshed before the burst-mode timer expires, the burst-mode timer will reset.

If the maximum allowable refresh time of the dynamic RAM is about to be exceeded, the burst mode timer will expire causing the $\overline{HOLD}$ pin to go low. This signals the CPU that a burst-mode refresh is manadatory and the burst-mode refresh will be accomplished when the CPU takes the REF REQ pins high. To ensure that all rows are refreshed, the address counter is reset to zero whenever the burst-mode timer expires. After the last row has been refreshed, the $\overline{HOLD}$ pin will return high, and the burst-mode timer will reset. The CPU can then return to normal transparent operation.

A LATCHED RCO output pin is also provided on the 'LS600A and 'LS601A to detect when the last row has been refreshed. Upon seeing a RCO from the address counter, the LATCHED RCO output will be set high. This latch is reset by providing a high-going pulse on the RESET LATCHED RCO input.

In the cycle-steal refresh mode ('LS602A or 'LS603A), refreshing is accomplished by dividing the safe refresh time into equal segments and refreshing one row in each segment. The segment time is programmed via the RC CYCLE STEAL input and will produce a low level on the $\overline{READY}$ output at the end of each segment period. This indicates to the CPU to suspend operations for one memory cycle for a row refresh. In effect it "steals" one memory cycle from the CPU. After the CPU recognizes the cycle-steal signal from the $\overline{READY}$ output, it must take both REF REQ pins high. These devices will then refresh one row and return control back to the CPU by taking $\overline{READY}$ high. The burst-mode timer is also provided to prevent exceeding the maximum allowable refresh time, and operates in the same manner as in the 'LS600A and 'LS601A. In applications where the burst-mode timer is not required, it can be disabled by connecting the RC Burst input to ground.

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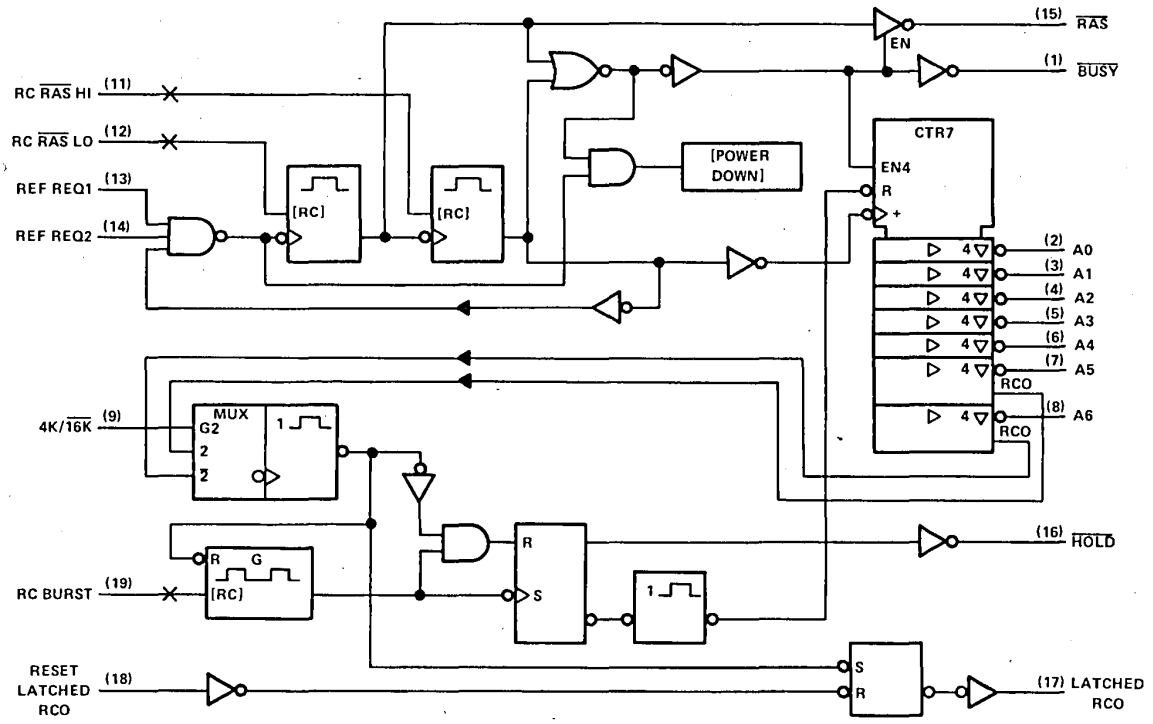
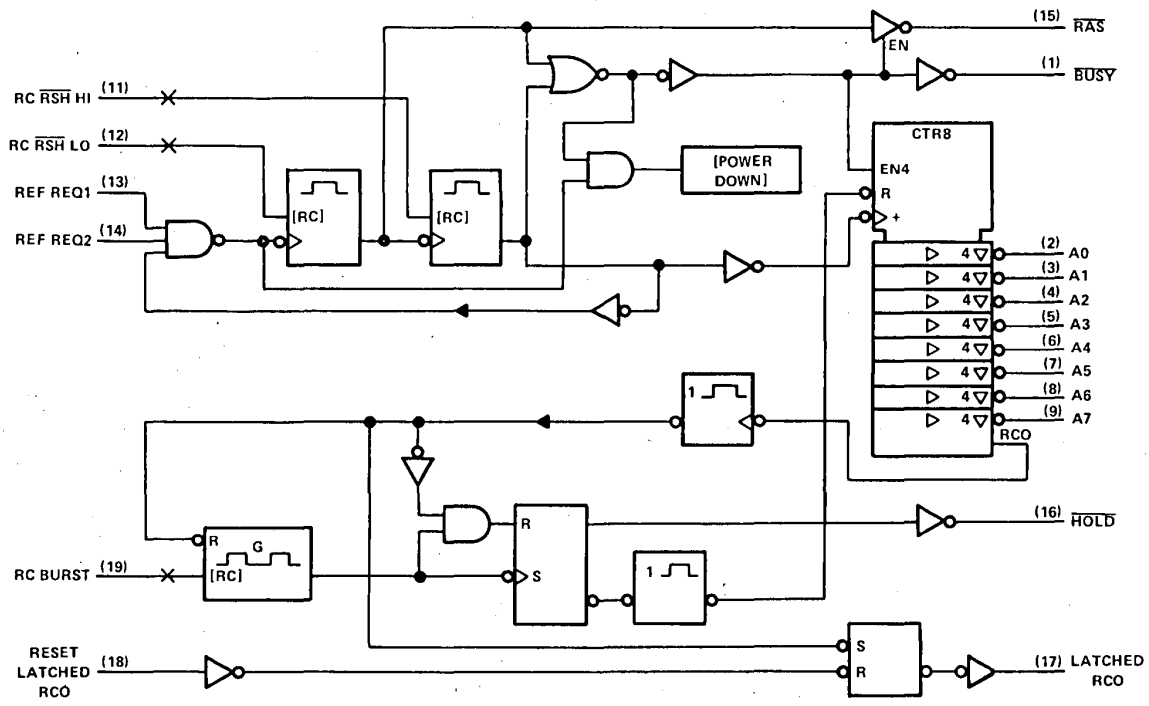
'LS600A



'LS601A



Pin numbers shown on logic notation are for DW, J or N packages.

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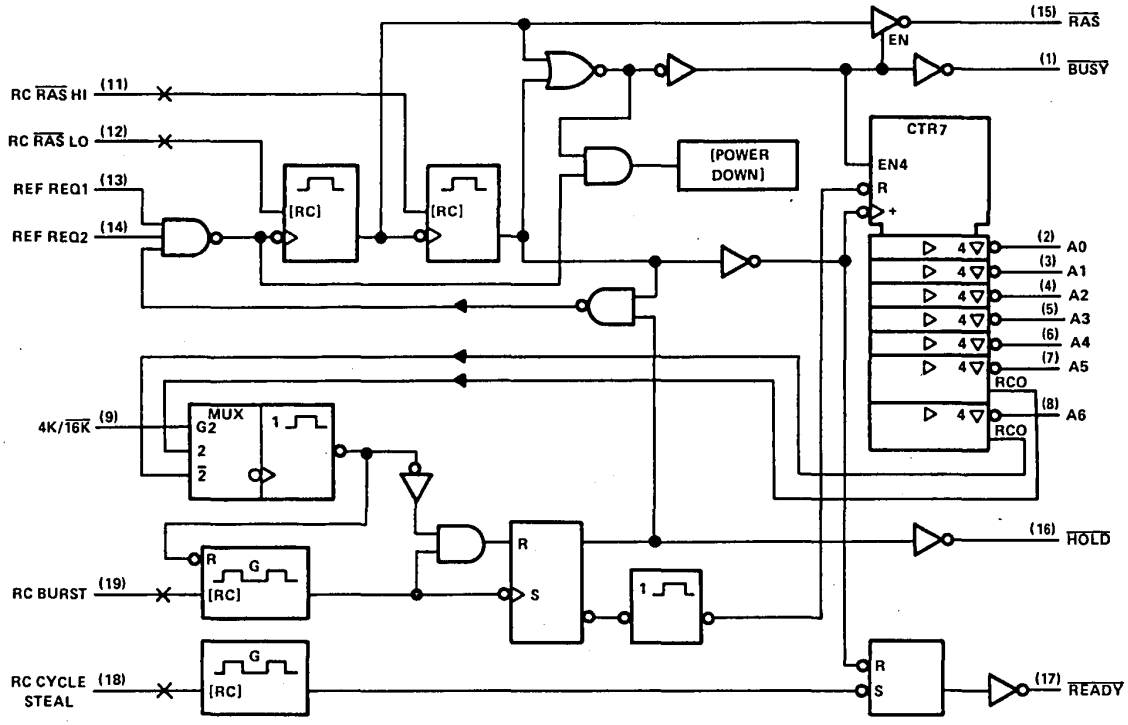
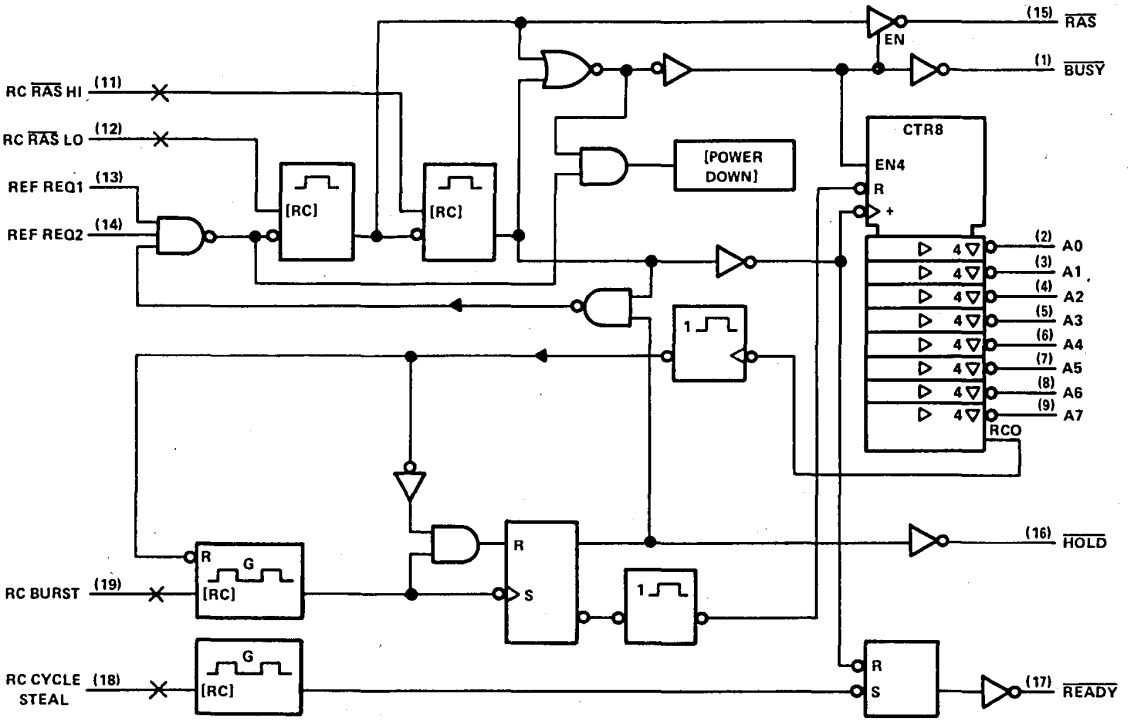
'LS602A



'LS603A



Pin numbers shown on logic notation are for DW, J or N packages.

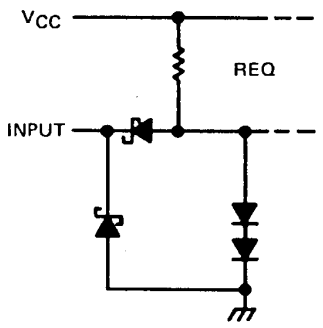
PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	$\overline{\text{BUSY}}$	Active output indicates to the CPU that a refresh cycle is in progress.
16	$\overline{\text{HOLD}}$	Active output should be a priority interrupt to the CPU for emergency burst refresh.
15	$\overline{\text{RAS}}$	3-state output row address strobe.
11	RC $\overline{\text{RAS}}$ HI	Timing node for high-level portion of $\overline{\text{RAS}}$. See Note 1.
12	RC $\overline{\text{RAS}}$ LO	Timing node for low-level portion of $\overline{\text{RAS}}$. See Note 1.
2-8	A0 thru A6	3-state output row address lines.
9	A7	MSB row address line for 'LS601A and 'LS603A (64K-bit memory controllers).
9	4K/$\overline{\text{16K}}$	A high input level disables the A5 row address line for 'LS600A and 'LS602A. (The high-level input makes the count chain 5 bits long while the low-level makes the count chain 6 bits long.)
17	$\overline{\text{READY}}$	Interrupt to CPU for cycle steal refresh ('LS602A and 'LS603A).
17	LATCHED RCO	Normally high-level, will latch low upon RCO of counter ('LS600A or 'LS601A).
18	RC CYCLE STEAL	Timing node that controls the $\overline{\text{READY}}$ output ('LS602A and 'LS603A). See Note 1.
18	RESET LATCHED RCO	Normally high-level, when pulsed low the LATCHED RCO output will be reset ('LS600A and 'LS601A).
19	RC BURST	Timing node for burst refresh. See Note 1.
13, 14	REF REQ1, REF REQ2	High level on both pins starts and continues row refresh. Low on either pin inhibits refresh.
20, 10	V_{CC}, GND	5-V power supply and network ground pins.

NOTE 1: All timing nodes require a resistor to V_{CC} and a capacitor to GND.

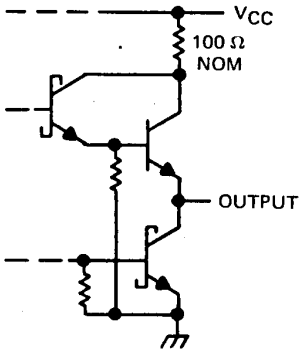
schematics of inputs and outputs

EQUIVALENT OF REF REQ, 4K/$\overline{\text{16K}}$, AND RESET LATCHED RCO INPUTS

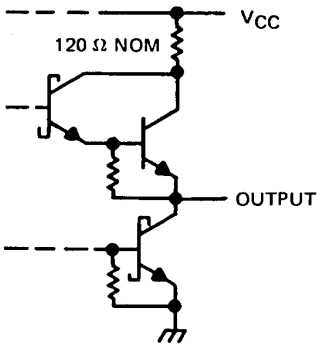


REF REQ: Req = 20 kΩ NOM
4K/$\overline{\text{16K}}$: Req = 30 kΩ NOM

TYPICAL OF $\overline{\text{RAS}}$ AND A OUTPUTS



TYPICAL OF $\overline{\text{BUSY}}$, $\overline{\text{HOLD}}$, $\overline{\text{READY}}$ AND LATCHED RCO OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 2: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	A, $\overline{RAS}$			−2.6	mA
	All others			−400	μA
Low-level output current, I_{OL}	A, $\overline{RAS}$			24	mA
	All others			8	
Duration or $\overline{RAS}$ output pulse†	High, t_{SHSL}	75			ns
	Low, t_{SLSH}	75			
Duration of RESET LATCHED RCO pulse, t_{RHRL}		35			ns
Duration of REF REQ pulse during CYCLE STEAL operation, t_{QHQL}		20			ns
External timing resistor, R_{ext}	RC $\overline{RAS}$ LO, RC $\overline{RAS}$ HI	1		6	kΩ
	RC BURST, RC CYCLE STEAL	1		1000	
Operating free-air temperature, T_A		0		70	°C

†Maximum operating frequency for the address counter corresponds to its minimum period, which is the sum of $t_{w(RAS-H)}$ min and $t_{w(RAS-L)}$ min.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, I_I = −1.8 mA				−1.5	V
V_{OH}	High-level output voltage	A, $\overline{RAS}$	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −2.6 mA	2.4	2.9		V
		All Others		I_{OH} = −400 μA	2.7	3.1		
V_{OL}	Low-level output voltage	A, $\overline{RAS}$	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA		0.25	0.4	V
				I_{OL} = 24 mA		0.35	0.5	
		All Others		I_{OL} = 4 mA		0.25	0.4	
				I_{OL} = 8 mA		0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	A, $\overline{RAS}$	V_{CC} = 5.25 V REF REQ at V_{IL} = 0.8 V	V_O = 2.7 V			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = 5.25 V,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current		V_{CC} = 5.25 V,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V,	V_I = 0.4 V			−0.4	mA
I_{OS}	Short-circuit output current§	A, $\overline{RAS}$	V_{CC} = 5.25 V		−30		−130	mA
		All others			−20		−100	
I_{CC}	Supply current		V_{CC} = 5.25 V, RC $\overline{RAS}$ LO and REF REQ at 0 V			50	85	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{QHBL}	REF REQ↑	$\overline{BUSY}$	C_L = 15 pF, R_L = 2 kΩ		30	45	ns
t_{SLBH}†	$\overline{RAS}$↓	$\overline{BUSY}$			245	300	ns
t_{QHSV}	REF REQ↑	$\overline{RAS}$	C_L = 320 pF, R_L = 667Ω		47	70	ns
t_{SHSZ}†	$\overline{RAS}$↑	$\overline{RAS}$	C_L = 5 pF, R_L = 667Ω		245	300	ns
t_{QHAV}	REF REQ↑	ADDRESS	C_L = 160 pF, R_L = 667Ω		38	65	ns
t_{SHAZ}†	$\overline{RAS}$↑	ADDRESS	C_L = 5 pF, R_L = 667Ω		245	300	ns
t_{RHCL}	RESET LATCHED RCO↑	LATCHED RCO	C_L = 15 pF, R_L = 2 kΩ		37	55	ns
t_{SHYH}	$\overline{RAS}$↑	$\overline{READY}$			64	85	ns
t_{SLSH}‡	$\overline{RAS}$↓	$\overline{RAS}$	C_L = 320 pF, R_L = 667Ω		210		ns
t_{SHSL}†	$\overline{RAS}$↑	$\overline{RAS}$			245		ns
t_{DHDL}§	$\overline{HOLD}$↑	$\overline{HOLD}$	C_L = 15 pF, R_L = 2 kΩ		3.56		ms
t_{YLYL}‖	$\overline{READY}$↑	$\overline{READY}$			27		μs

† Depends on RC network at pin 11 (4 kΩ, 200 pF used for testing).
‡ Depends on RC network at pin 12 (4 kΩ, 200 pF used for testing).
§ Depends on RC network at pin 19 (680 kΩ, 0.022 μF used for testing).
‖ Depends on RC network at pin 18 (10 kΩ, 0.01 μF used for testing).
NOTE 3: See General Information Section for load circuits and voltage waveforms.

explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A or C SUBSCRIPT
$\overline{BUSY}$	B
$\overline{HOLD}$	D
$\overline{RAS}$	S
A0 – A7	A
$\overline{READY}$	Y
LATCHED RCO	C
RESET LATCHED RCO	R
REF REQ	Q

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TIMING DIAGRAMS

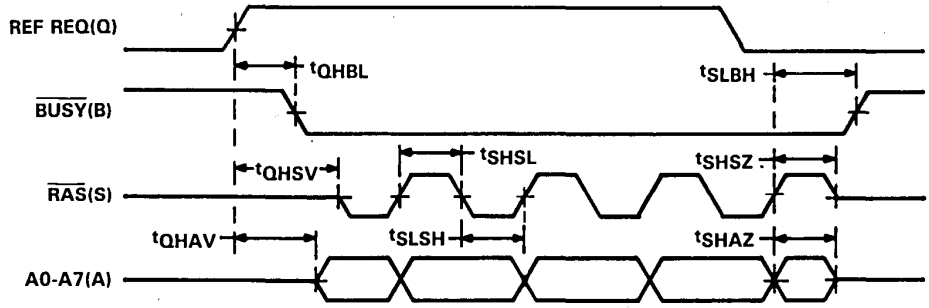


FIGURE 1 – TRANSPARENT REFRESH

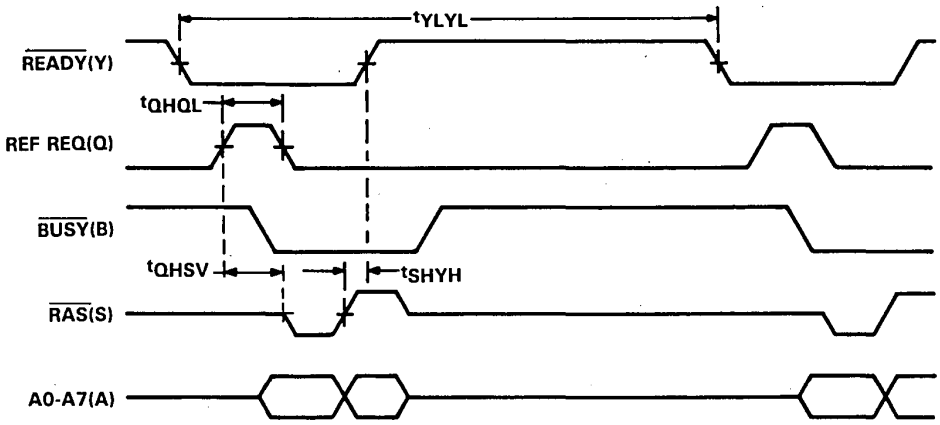
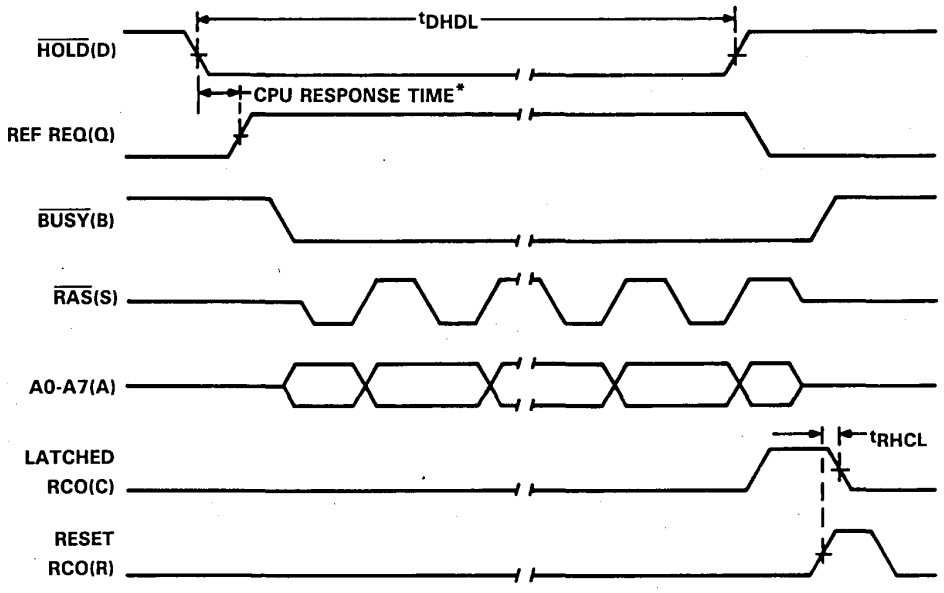


FIGURE 2 – CYCLE STEAL REFRESH



* During testing, an 'LS04 is used to invert $\overline{\text{HOLD}}$ to provide the REF REQ input.

FIGURE 3 – BURST MODE REFRESH

TYPICAL CHARACTERISTICS

PULSE DURATION, $\overline{RAS}$ LOW
vs
EXTERNAL TIMING RESISTOR

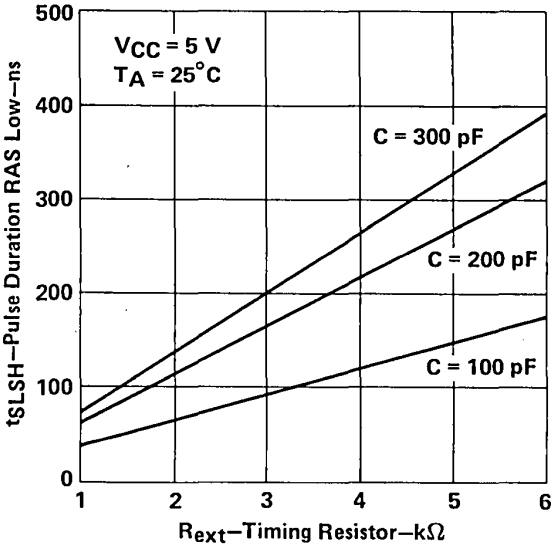


FIGURE 4

CYCLE STEAL REFRESH CYCLE TIME
vs
EXTERNAL TIMING RESISTOR

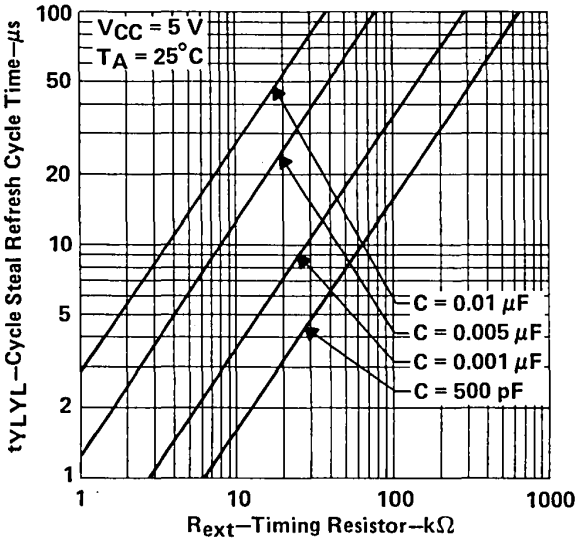


FIGURE 5

PULSE DURATION, RAS HIGH
vs
EXTERNAL TIMING RESISTOR

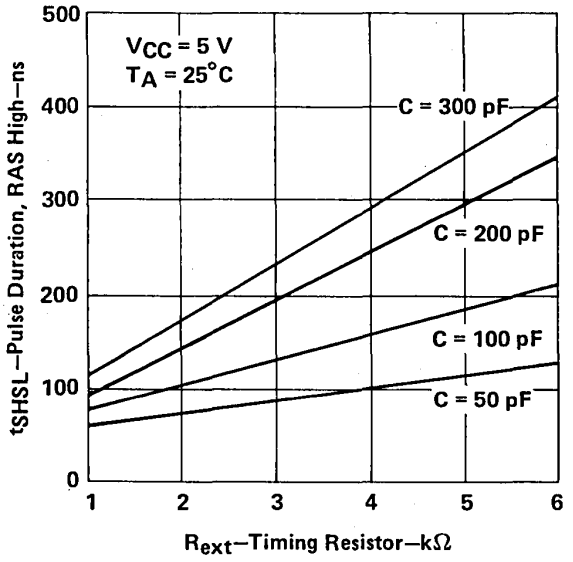


FIGURE 6

PULSE DURATION, BURST REFRESH
vs
EXTERNAL TIMING RESISTOR

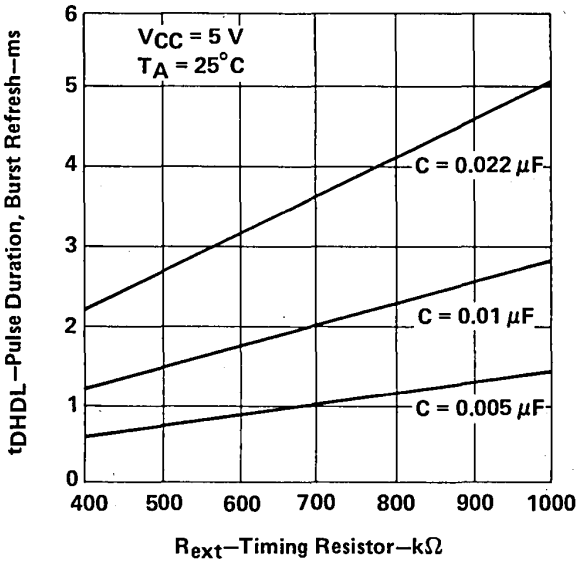


FIGURE 7

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