

TYPES SN54LS608, SN74LS608 (TIM99608) MEMORY CYCLE CONTROLLERS

D2548, JANUARY 1981 — REVISED DECEMBER 1981

- Provides Correct Timing for Memory Cycles
 - Read Cycle
 - Write Cycle
 - Read-Modify-Write Cycle
 - RAS-Only Refresh Cycle
- Page or Normal Modes
- Stand-Alone Controller for CPU-to-Memory Interface
- Also Designed to be Part of a Three-Chip Set Consisting of 'LS600 thru 'LS603, 'LS604 thru 'LS607, and 'LS608
- RAS Output is 3-State to Share Bus With 'LS600 thru 'LS603
- Critical Times Are User RC-Programmable to Optimize System Performance

description

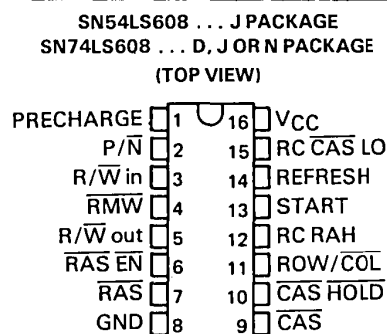
The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

The 'LS608 can operate as a stand-alone interface but it is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

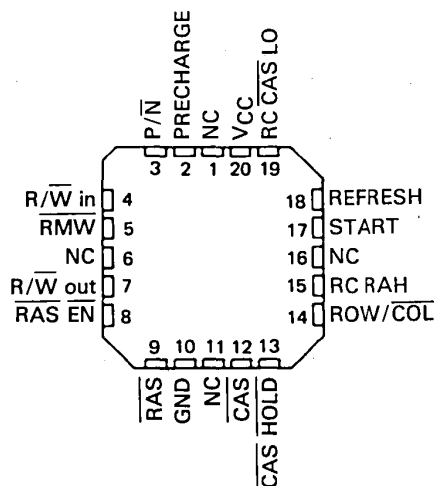
After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper RAS, CAS, and READ/WRITE output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

| MEMORY CYCLE | MODE | INPUT CONDITIONS | | | | | | |
|-------------------|---------|------------------|-----------------|----------------------|---------------|-------------|----------|------------|
| | | P/ \bar{N} IN | R/ \bar{W} IN | $\bar{R}M\bar{W}$ IN | RAS ENABLE IN | CAS HOLD IN | START IN | REFRESH IN |
| READ | PAGE | H | H | H | L | H | ↑ | L |
| WRITE | | H | L | H | L | H | ↑ | L |
| READ-MODIFY-WRITE | | H | H | L | L | H | ↑ | L |
| READ | NORMAL | L | H | H | L | H | ↑ | L |
| WRITE | | L | L | H | L | H | ↑ | L |
| READ-MODIFY-WRITE | | L | H | L | L | H | ↑ | L |
| REFRESH | REFRESH | x | x | x | L | H | ↑ | H |
| EXTERNAL REFRESH | | x | x | x | H | H | x | L |

H = High, L = Low, x = Irrelevant, ↑ = low-to-high transition



SN54LS608 ... FK PACKAGE
SN74LS608 ... FN PACKAGE
(TOP VIEW)



NC — No internal connection

3
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PRODUCTION DATA

This document contains information current as of publication date. Products conform to these specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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MEMORY CYCLE CONTROLLERS**

PIN FUNCTION TABLE

| PIN | PIN NAME | FUNCTIONAL DESCRIPTION |
|-----|---|---|
| 1 | RC PRECHARGE | User-programmable timing node* for precharge ($\overline{\text{CAS}}$ high and $\overline{\text{RAS}}$ high). |
| 2 | $\text{P}/\overline{\text{N}}$ IN | When high, initiates a ready cycle (holds R/W OUT high) and, when low, page mode read or write cycle holds $\overline{\text{RAS}}$ continuously low while $\overline{\text{CAS}}$ and column addresses are sequenced. |
| 3 | $\text{R}/\overline{\text{W}}$ IN | When high, initiates a ready cycle (holds $\text{R}/\overline{\text{W}}$ OUT high) and, when low, initiates a write cycle (holds $\text{R}/\overline{\text{W}}$ OUT low) if pin 4 is high and pin 14 is low. |
| 4 | $\overline{\text{RMW}}$ IN | When low, enables read-modify-write cycle. $\text{R}/\overline{\text{W}}$ IN must be high at the start of the RMW cycle. |
| 5 | $\text{R}/\overline{\text{W}}$ OUT | When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally ties to a $\overline{\text{W}}$ memory input in a system. |
| 6 | $\overline{\text{RAS}}$ ENABLE IN | When low, enables $\overline{\text{RAS}}$ output. When high, $\overline{\text{RAS}}$ is in the high-impedance or third state. |
| 7 | $\overline{\text{RAS}}$ OUT | 3-state row-address-strobe output controlled by $\overline{\text{RAS}}$ ENABLE IN. In the three-chip controller set, the $\overline{\text{RAS}}$ output of the 'LS608 ties to the $\overline{\text{RAS}}$ output of the refresh controller ('LS600 thru 'LS603). |
| 8 | GND | Device and substrate ground. |
| 9 | $\overline{\text{CAS}}$ OUT | Column-address-strobe output. |
| 10 | $\overline{\text{CAS}}$ HOLD IN | When low, allows $\overline{\text{CAS}}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle. |
| 11 | ROW/ $\overline{\text{COL}}$ (or $\overline{\text{MEMBSY}}$) OUT | In a system where the 'LS608 is a stand-alone controller, this output indicates a memory-busy condition to the microprocessor. When the 'LS608 is used as a part of a three-chip controller set, this pin ties to the SELECT A/ $\overline{\text{B}}$ input of the multiplexer ('LS604 thru 'LS607) for selecting row and column in addition to indicating a memory-busy condition to the microprocessor. |
| 12 | RC RAH | User-programmable timing node* for row address hold time. (high level at ROW/ $\overline{\text{COL}}$ OUT). |
| 13 | START IN | When changed from low to high, initiates a memory cycle. |
| 14 | REFRESH IN | When high, enables $\overline{\text{RAS}}$ -only refresh cycle. |
| 15 | RC $\overline{\text{CAS}}$ LO | User-programmable timing node* for column-address-strobe low time. |
| 16 | V _{CC} | 5-volt power supply terminal. |

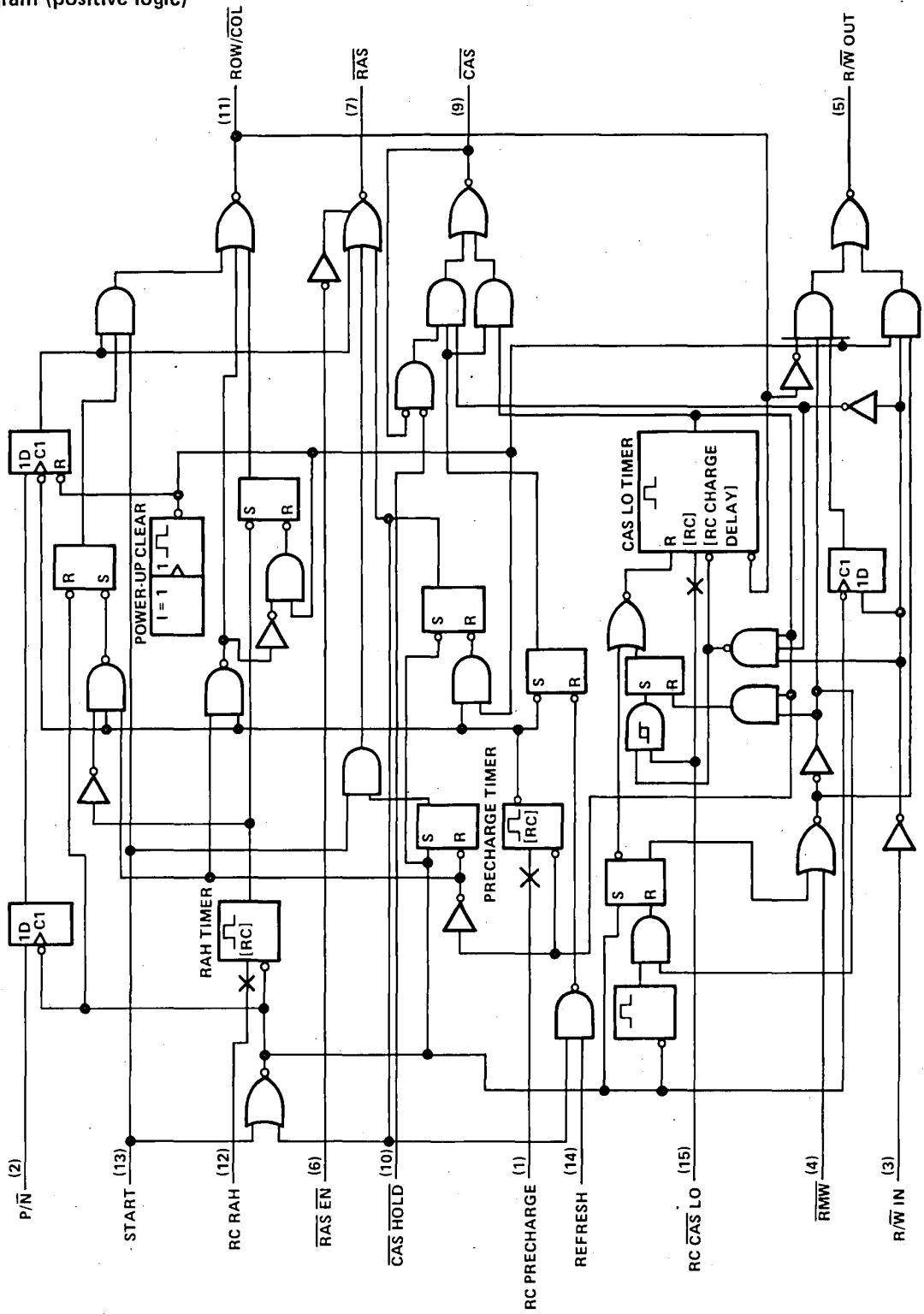
*All timing nodes require a resistor to V_{CC} and a capacitor to ground. Programmed time is approximately 0.29 RC.

3

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TYPES SN54LS608, SN74LS608
MEMORY CYCLE CONTROLLERS

logic diagram (positive logic)

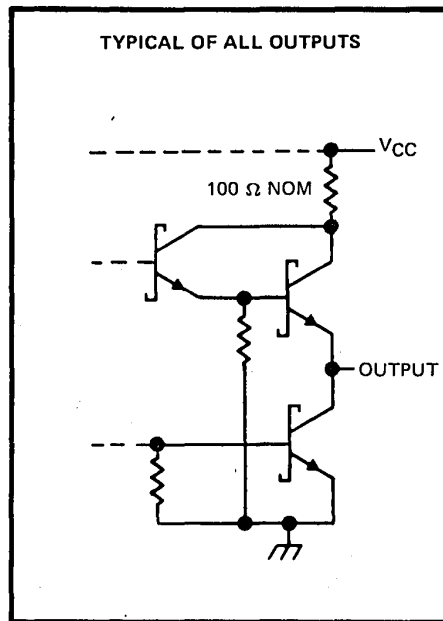
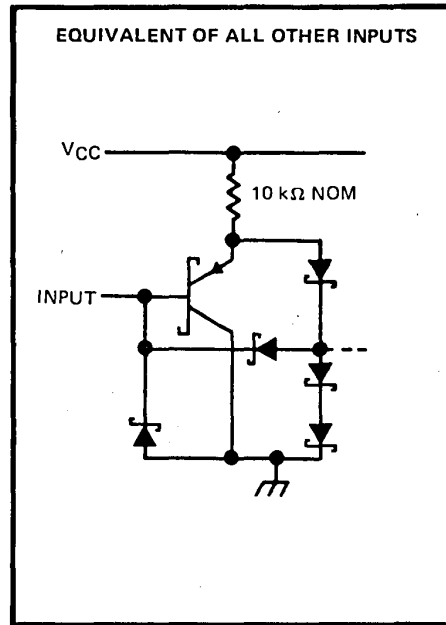
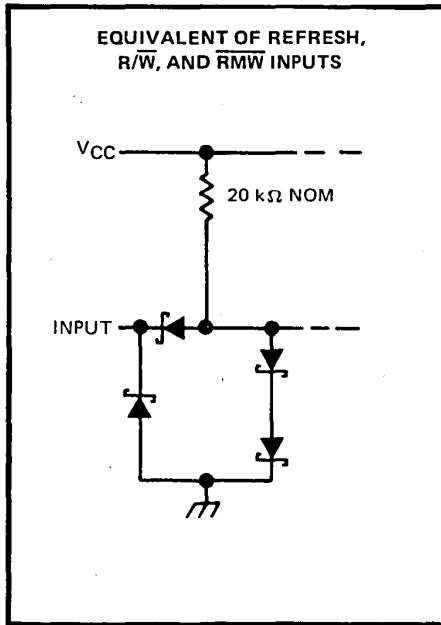


Pin numbers shown on logic notation are for D, J, or N packages.

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**TYPES SN54LS608, SN74LS608
MEMORY CYCLE CONTROLLERS**

schematics of inputs and outputs



3

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TYPES SN54LS608, SN74LS608 MEMORY CYCLE CONTROLLERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1)..... | 7 V |
| Input voltage..... | 7 V |
| Off-state output voltage..... | 5.5 V |
| Operating free-air temperature range: SN54LS608..... | -55°C to 125°C |
| SN74LS608..... | 0°C to 70°C |
| Storage temperature range..... | -65°C to 150°C |

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

| | | SN54LS608 | | | SN74LS608 | | | UNIT |
|-----------|--------------------------------|--------------------------------------|-----|------|-----------|------|------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.8 | | | V |
| I_{OH} | High-level output current | ROW/COL | | -0.4 | | -0.4 | | mA |
| | | RAS | | -1 | | -2.6 | | |
| | | All others | | -1.2 | | -1.2 | | |
| I_{OL} | Low-level output current | ROW/COL | | 4 | | 8 | | mA |
| | | All others | | 12 | | 24 | | |
| t_{su} | Setup time | R/W, RMW, P/N, or REFRESH to START † | | 20 | | 20 | | ns |
| | | CAS HOLD to CAS ↓ | | 20 | | 20 | | |
| t_h | Hold time | 0 | | | 0 | | | ns |
| R_{ext} | External timing resistor | RC RAH | | 0.1 | | 2 | | kΩ |
| | | RC CAS LO, RC PRECHARGE | | 1 | | 6 | | |
| T_A | Operating free-air temperature | -55 | | 125 | | 0 | | 70 |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54LS608 | | | SN74LS608 | | | UNIT | |
|-----------|--|--|-------------------------------|------|-----------|------|------|------|----|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | | |
| V_{IK} | $V_{CC} = \text{MIN}$ $I_I = -18 \text{ mA}$ | -1.5 | | | -1.5 | | | V | |
| V_{OH} | ROW/COL | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$ | $I_{OH} = -400 \mu\text{A}$ | 2.5 | 3.4 | 2.7 | 3.4 | V | |
| | RAS | | $I_{OH} = \text{MAX}$ | 2.4 | 3.2 | 2.4 | 3.1 | | |
| | Others | | $I_{OH} = -1.2 \text{ mA}$ | 2.4 | 3.2 | 2.4 | 3.2 | | |
| V_{OL} | ROW/COL | $V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = \text{MAX}$ | $I_{OL} = 4 \text{ mA}$ | 0.25 | | 0.4 | | V | |
| | Others | | $I_{OL} = 8 \text{ mA}$ | | | 0.35 | | | |
| | | | $I_{OL} = 12 \text{ mA}$ | 0.25 | | 0.4 | | | |
| | $I_{OL} = 24 \text{ mA}$ | | | | 0.35 | | 0.5 | | |
| I_{OZH} | RAS | $V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 2.7 \text{ V}$ | | | 20 | | μA | | |
| I_{OZL} | RAS | $V_{CC} = \text{MAX}$, $V_{IH} = 2 \text{ V}$, $V_O = 0.4 \text{ V}$ | | | -20 | | μA | | |
| I_I | | $V_{CC} = \text{MAX}$, $V_I = 7 \text{ V}$ | | | 0.1 | | mA | | |
| I_{IH} | | $V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$ | | | 20 | | μA | | |
| I_{IL} | REFRESH, R/W, RMW | $V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$ | | | -0.4 | | mA | | |
| | Others | | | | -0.2 | | | | |
| | | | | | -0.2 | | | | |
| I_O | ROW/COL | $V_{CC} = \text{MAX}$ | $V_O = 2.25 \text{ V}$ | -10 | -50 | -10 | -50 | mA | |
| | Others | | $V_O = 0 \text{ V} \text{ §}$ | -30 | -130 | -30 | -130 | | |
| I_{CC} | | $V_{CC} = \text{MAX}$, Outputs open, All inputs at GND | 38 | | 65 | | 38 | 65 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

3

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TYPES SN54LS608, SN74LS608 MEMORY CYCLE CONTROLLERS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$ to GND (see waveforms for more detail)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MODE | MIN | TYP | MAX | UNIT | |
|--------------------|---|-------------------------|--------------------------------------|-------------|-----|-----|-----|------|----|
| t_{PHL} | START \uparrow | $\overline{\text{RAS}}$ | $R_L = 667\ \Omega$ to V_{CC} | NORMAL READ | 8 | 15 | | ns | |
| t_{PLH}^\dagger | START \uparrow | $\overline{\text{RAS}}$ | | | 290 | 363 | 435 | | ns |
| t_{PHL}^\ddagger | START \uparrow | $\overline{\text{CAS}}$ | | | 100 | 126 | 150 | | ns |
| t_{PLH}^\ddagger | START \uparrow | $\overline{\text{CAS}}$ | | | 275 | 342 | 410 | | ns |
| t_{PHL}^\ddagger | START \uparrow | R/W | | | 90 | 113 | 135 | | ns |
| t_{PLH}^\ddagger | START \uparrow | R/W | | | 303 | 383 | 460 | | ns |
| t_{PLH} | CAS HOLD \uparrow | CAS | $R_L = 2\text{ k}\Omega$ to V_{CC} | NORMAL READ | 10 | 15 | | ns | |
| t_{PHL}^\ddagger | START \uparrow | ROW/COL | | | 75 | 100 | 125 | | ns |
| t_{PLH}^\ddagger | START \uparrow | ROW/COL | | | 485 | 609 | 730 | | ns |
| t_{PHL} | R/W \downarrow | R/W | $R_L = 667\ \Omega$ to V_{CC} | NORMAL RMW | 13 | 20 | | ns | |
| t_{PLH} | ROW/COL \uparrow | R/W | | | 10 | 15 | | | ns |
| t_{PLH} | RMW \uparrow | $\overline{\text{CAS}}$ | | | 34 | 50 | | | ns |
| t_{PLH}^\diamond | RMW \uparrow | ROW/COL | | | 240 | 300 | 360 | | ns |
| t_{PZH} | $\overline{\text{RAS}}\text{ EN}\downarrow$ | $\overline{\text{RAS}}$ | $R_L = 667\ \Omega$ to GND | NORMAL READ | 13 | 20 | | ns | |
| t_{PZL} | $\overline{\text{RAS}}\text{ EN}\downarrow$ | $\overline{\text{RAS}}$ | $R_L = 667\ \Omega$ to V_{CC} | | 14 | 25 | | ns | |
| t_{PHZ} | $\overline{\text{RAS}}\text{ EN}\uparrow$ | $\overline{\text{RAS}}$ | $R_L = 667\ \Omega$ to GND | | 7 | 15 | | ns | |
| t_{PLZ} | $\overline{\text{RAS}}\text{ EN}\uparrow$ | $\overline{\text{RAS}}$ | $R_L = 667\ \Omega$ to V_{CC} | | 16 | 25 | | ns | |

† Depends on RC network at pin 12 (2 k Ω , 180 pF used for testing) and the RC network at pin 15 (5 k Ω , 180 pF).

‡ Depends on RC network at pin 12 (2 k Ω , 180 pF).

§ Depends on RC networks at pin 12 (2 k Ω , 180 pF), pin 15 (5 k Ω , 180 pF), and pin 1 (5 k Ω , 180 pF).

$^\diamond$ Depends on RC network at pin 1 (5 k Ω , 180 pF).

NOTE 2: Measurement point for all t_{PHZ} output pulses is 2.9 V. Measurement point for all t_{PLZ} output pulses is 0.8 V. All other measurement points are 1.3 V.

3

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PARAMETER MEASUREMENT INFORMATION

