

# TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

D2549, JANUARY 1981 — REVISED DECEMBER 1983

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS 9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

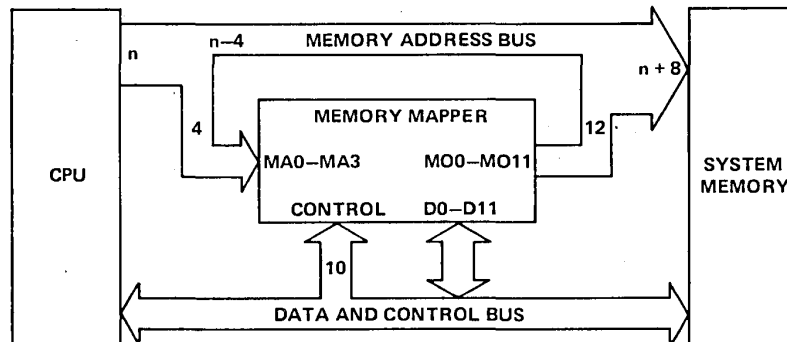
## description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see the figure below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of  $2^{(n-4)}$  registers each without reloading ( $n$  = number of address bits available from CPU.)

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/W whenever chip select (CS) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when CS is high and MM (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When CS and MM are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8-MO11, respectively, (assuming appropriate latch control) with low levels in the other bit positions on the map outputs.



## PRODUCTION DATA

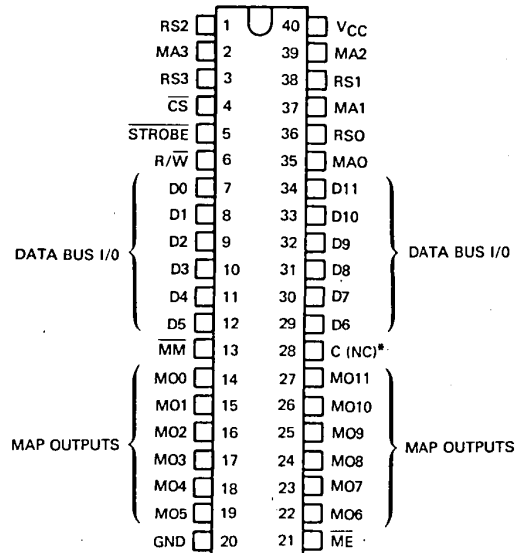
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS INSTRUMENTS**

POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

3-1187

(TIM99610 THRU TIM99613) SN54LS'... JD PACKAGE  
SN74LS'... JD OR N PACKAGE  
(TOP VIEW)



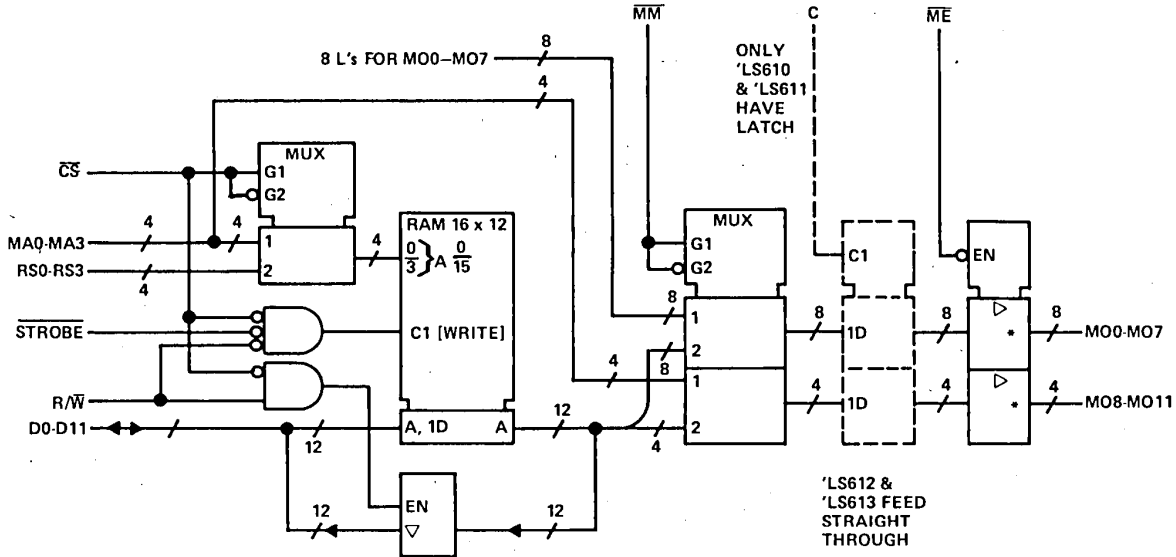
\*Note: Pin 28 has no internal connection on 'LS612 and 'LS613  
For chip carrier information, contact the factory.

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# TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

functional block diagram (positive logic)



\*'LS610 and 'LS612 have 3-state ( $\nabla$ ) map outputs.  
'LS611 and 'LS613 have open-collector ( $\Omega$ ) map outputs.

PIN FUNCTION TABLE

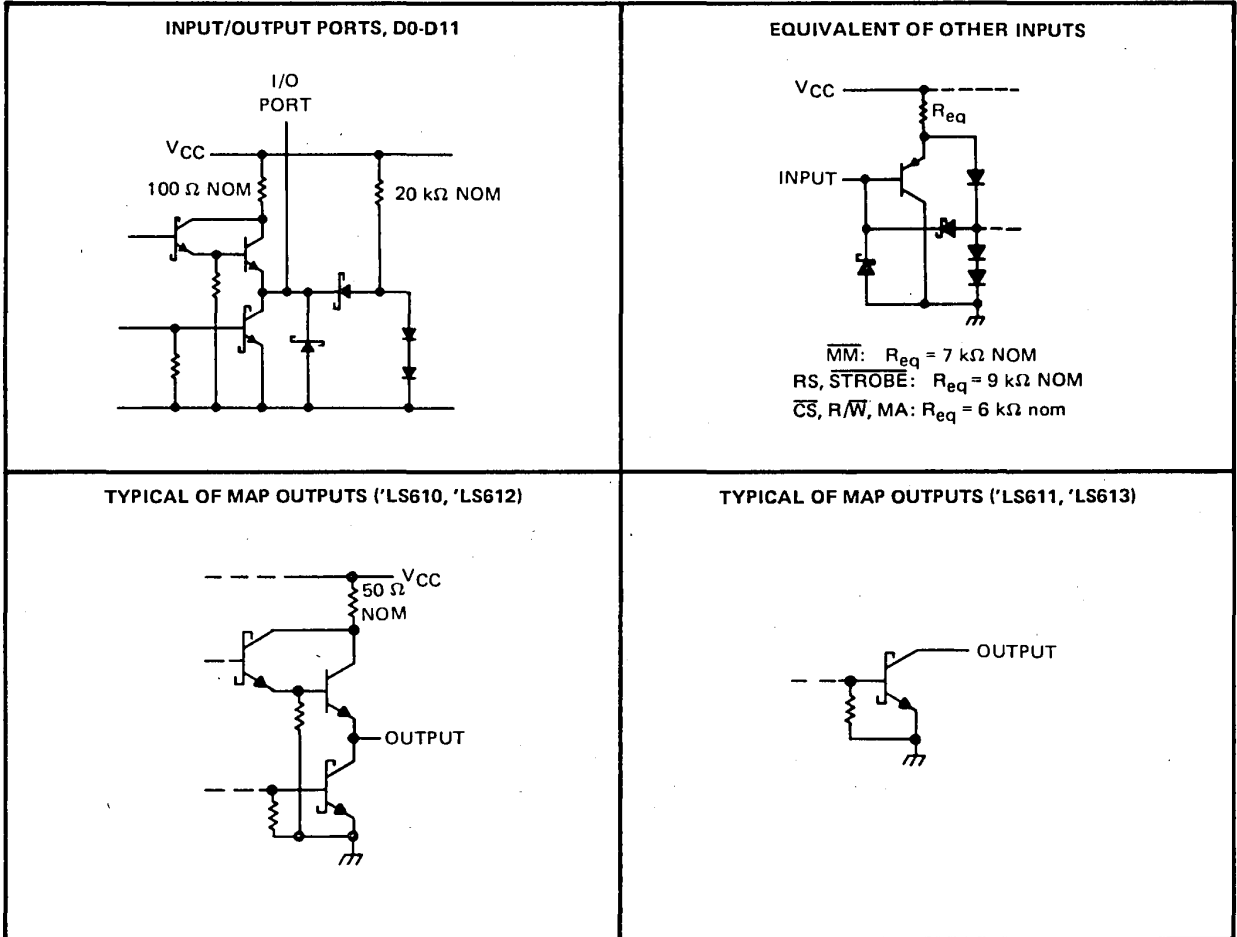
PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7-12, 29-34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0-RS3 when $\overline{CS}$ is low. Mode controlled by R/W.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/W	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	STROBE	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ( $\overline{MM}$ low and $\overline{CS}$ high).
14-19, 22-27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8-MO11 and low levels on MO0-MO7.
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	VCC, GND	5-V power supply and network ground (substrate) pins.

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# TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

## schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: Data Bus I/O	5.5 V
All other inputs	7 V
Operating free-air temperature range: SN54LS610 through SN54LS613	-55°C to 125°C
SN74LS610 through SN74LS613	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# TYPES SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

## recommended operating conditions

			SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
I <sub>OH</sub>	High-level output current	MO			-12			-15	mA		
		D			-1			-2.6			
I <sub>OL</sub>	Low-level output current	MO			12			24	mA		
		D			4			8			
t <sub>AVCL</sub>	C setup time (AV before C low)	'LS610 only	See Figure 2			30			ns		
t <sub>SLSH</sub>	Width of strobe input pulse		75			75			ns		
t <sub>CSSL</sub>	$\overline{CS}$ setup ( $\overline{CS}$ low to strobe low)		20			20			ns		
t <sub>WLSL</sub>	R/W setup time (R/W low to strobe low)		20			20			ns		
t <sub>RVSL</sub>	RS setup time (RS valid to strobe low)		20			20			ns		
t <sub>DVSH</sub>	Data setup time (D0-D11 valid to strobe high)		75			75			ns		
t <sub>SHCSH</sub>	$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high)		20			20			ns		
t <sub>SHWH</sub>	R/W hold time (Strobe high to R/W high)		20			20			ns		
t <sub>SHRX</sub>	RS hold time (Strobe high to RS invalid)		20			20			ns		
t <sub>SHDX</sub>	Data hold time (Strobe high to D0-D11 invalid)		20			20			ns		
T <sub>A</sub>	Operating free-air temperature		-55			125			0	70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IH</sub>	High-level input voltage		2			2			V	
V <sub>IL</sub>	Low-level input voltage		0.7			0.8			V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V	
V <sub>OH</sub>	High-level output voltage	MO D	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OH</sub> = -3 mA	2.4		2.4		V	
				I <sub>OH</sub> = MAX	2		2			
V <sub>OL</sub>	Low-level output voltage	MO	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V	
				I <sub>OL</sub> = 24 mA			0.35 0.5			
		D		I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4		
				I <sub>OL</sub> = 8 mA			0.35 0.5			
I <sub>OZH</sub>	Off-state output current, high-level voltage applied		20			20			µA	
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	MO	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, V <sub>O</sub> = 0.4 V			-20			µA	
		D				-400				
I <sub>I</sub>	Input current at maximum input voltage	D	V <sub>CC</sub> = MAX			100			µA	
		All others	V <sub>I</sub> = 5.5 V			100				
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			µA	
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4			mA	
I <sub>OS</sub>	Short-circuit output current§	MO	V <sub>CC</sub> = MAX			-40	-225	-40	-225	mA
		D				-30	-130	-30	-130	
I <sub>CC</sub>	Supply current		V <sub>CC</sub> = MAX	Outputs high	112	180	112	180	mA	
				Outputs low	112	180	112	180		
				Outputs at high impedance	150	230	180	230		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

# TYPES SN54LS610, SN54LS612, SN74LS610, SN74LS612 MEMORY MAPPERS WITH 3-STATE MAP OUTPUTS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 45\text{ pF}$  to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$t_{CSLDV}$ Access (enable) time	$\overline{CS}\downarrow$	D 0-11	$R_L = 2\text{ k}\Omega$ See Figure 1, See Notes 3 and 4	28	50		26	50	ns	
$t_{WHDV}$ Access (enable) time	$R/\overline{W}\uparrow$	D 0-11		20	35		20	35	ns	
$t_{RVDV}$ Access time	RS	D 0-11		49	75		39	75	ns	
$t_{WLDZ}$ Disable time	$R/\overline{W}\downarrow$	D 0-11		32	50		30	50	ns	
$t_{CSHDZ}$ Disable time	$\overline{CS}\uparrow$	D 0-11	$R_L = 667\ \Omega$ ; See Figure 2, See Notes 3 and 4	42	65		38	65	ns	
$t_{ELQV}$ Access (enable) time	$\overline{ME}\downarrow$	MO 0-11		19	30		17	30	ns	
$t_{CSHQV}$ Access time	$\overline{CS}\uparrow$	MO 0-11		56	85		48	85	ns	
$t_{MLQV}$ Access time	$\overline{MM}\downarrow$	MO 0-11		25	40		22	40	ns	
$t_{CHQV}$ Access time	$C\uparrow$	MO 0-11		24	40				ns	
$t_{AVQV1}$ Access time (MM low)	MA	MO 0-11		46	70		39	70	ns	
$t_{MHQV}$ Access time	$\overline{MM}\uparrow$	MO 0-11		24	40		22	40	ns	
$t_{AVQV2}$ Propagation time (MM high)	MA	MO 8-11		19	30		13	30	ns	
$t_{EHQZ}$ Disable time	$\overline{ME}\uparrow$	MO 0-11		14	25		14	25	ns	

NOTE: 3. Access times are tested as  $t_{PLH}$  and  $t_{PHL}$  or  $t_{pZH}$  or  $t_{pZL}$ . Disable times are tested as  $t_{PHZ}$  and  $t_{PLZ}$ .  
4. See General Information Section for load circuits and voltage waveforms.

### explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

$t_{AB-CD}$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

- H = high or transition to high
- L = low or transition to low
- V = a valid steady-state level
- X = unknown, changing, or "don't care" level
- Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A AND C- SUBSCRIPT
C	C
$\overline{CS}$	CS
D0-11	D
MA0-MA3	A
MO0-MO11	O
$\overline{ME}$	E
$\overline{MM}$	M
R/ $\overline{W}$	W
RS0-RS3	R
STROBE	S

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# TYPES SN54LS611, SN54LS613, SN74LS611, SN74LS613 MEMORY MAPPERS WITH OPEN-COLLECTOR MAP OUTPUTS

## recommended operating conditions

				SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT	
				MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage			4.5	5	5.5	4.75	5	5.25	V	
V <sub>OH</sub>	High-level output voltage			5.5			5.5			V	
I <sub>OH</sub>	High-level output current			-1			-2.6			mA	
I <sub>OL</sub>	Low-level output current			MO			24			mA	
				D			8				
t <sub>AVCL</sub>	C setup time (AV before C low)	'LS611 only	See Figure 2		30	30		ns			
t <sub>SLSH</sub>	Width of strobe input pulse			75		75		ns			
t <sub>CSSL</sub>	CS setup time (CS low to strobe low)			20		20		ns			
t <sub>WLSL</sub>	R/W setup time (R/W low to strobe low)			20		20		ns			
t <sub>RVSL</sub>	RS setup time (RS valid to strobe low)			20		20		ns			
t <sub>DVSH</sub>	Data setup time (D0-D11 valid to strobe high)			75		75		ns			
t <sub>SHCSH</sub>	CS hold time (Strobe high to CS high)			20		20		ns			
t <sub>SHWH</sub>	R/W hold time (Strobe high to R/W high)			20		20		ns			
t <sub>SHRX</sub>	RS hold time (Strobe high to RS invalid)			20		20		ns			
t <sub>SHDX</sub>	Data hold time (Strobe high to D0-D11 invalid)			20		20		ns			
T <sub>A</sub>	Operating free-air temperature			-55		125		0		70	°C

NOTE 2: Voltage values are with respect to network ground terminal.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT	
				MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IH</sub>	High-level input voltage				2		2		V		
V <sub>IL</sub>	Low-level input voltage				0.7		0.8		V		
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5		-1.5		V		
V <sub>OH</sub>	High-level output voltage	D	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OH</sub> = MAX		2.4		2.4				
I <sub>OH</sub>	High-level output current		MO		100		100		μA		
V <sub>OL</sub>	Low-level output voltage	MO	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 12 mA		0.25	0.4	0.25	0.4	V		
			I <sub>OL</sub> = 24 mA				0.35 0.5				
		D	V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OL</sub> = 4 mA		0.25	0.4	0.25	0.4			
			I <sub>OL</sub> = 8 mA				0.35 0.5				
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	D	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, V <sub>O</sub> = 2.7 V		20		20		μA		
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	D	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.4 V		-400		-400				
I <sub>I</sub>	Input current at maximum input voltage	D	V <sub>CC</sub> = MAX		100		100				
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20		20				
I <sub>IL</sub>	Low-level input current		V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4		-0.4		mA		
I <sub>OS</sub>	Short-circuit output current§	D	V <sub>CC</sub> = MAX		-30	-130	-30	-130	mA		
I <sub>CC</sub>	Supply current		V <sub>CC</sub> = MAX		Outputs high		100	170	100	170	mA
					Outputs low		100	170	100	170	
					Outputs at high impedance		110	200	110	200	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

## TYPES SN54LS611, SN54LS613, SN74LS611, SN74LS613 MEMORY MAPPERS WITH OPEN-COLLECTORS OUTPUTS

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 45\text{ pF}$  to GND

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS611			'LS613			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tCSLDV Access (enable) time	$\overline{CS}\downarrow$	D 0-11	$R_L = 2\text{ k}\Omega$ , See Figure 1, See Notes 3 and 4	31	50		28	50	ns	
tWHDV Access (enable) time	$R/\overline{W}\uparrow$	D 0-11		23	35		21	35	ns	
tRVDV Access time	RS	D 0-11		51	75		47	75	ns	
tWLDZ Disable time	$R/\overline{W}\downarrow$	D 0-11		32	50		31	50	ns	
tCSHDZ Disable time	$\overline{CS}\uparrow$	D 0-11		41	65		40	65	ns	
tELQV Access (enable) time	$\overline{ME}\downarrow$	MO 0-11	$R_L = 667\ \Omega$ , See Figure 2, See Notes 3 and 4	21	30		19	30	ns	
tCSHQV Access time	$\overline{CS}\uparrow$	MO 0-11		57	90		53	90	ns	
tMLQV Access time	MM $\downarrow$	MO 0-11		25	40		25	40	ns	
tCHQV Access time	C $\uparrow$	MO 0-11		30	45				ns	
tAVQV1 Access time (MM low)	MA	MO 0-11		47	70		44	70	ns	
tMHQV Access time	MM $\uparrow$	MO 0-11		31	50		31	50	ns	
tAVQV2 Propagation time (MM high)	MA	MO 8-11		21	30		20	30	ns	
tEHQZ Disable time	$\overline{ME}\uparrow$	MO 0-11		15	25		15	25	ns	

NOTE: 3. Access times are tested as  $t_{PLH}$  and  $t_{PHL}$  or  $t_{PZH}$  or  $t_{PZL}$ . Disable times are tested as  $t_{PHZ}$  and  $t_{PLZ}$ .  
4. See General Information Section for load circuits and voltage waveforms.

TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613  
MEMORY MAPPERS

TIMING DIAGRAMS

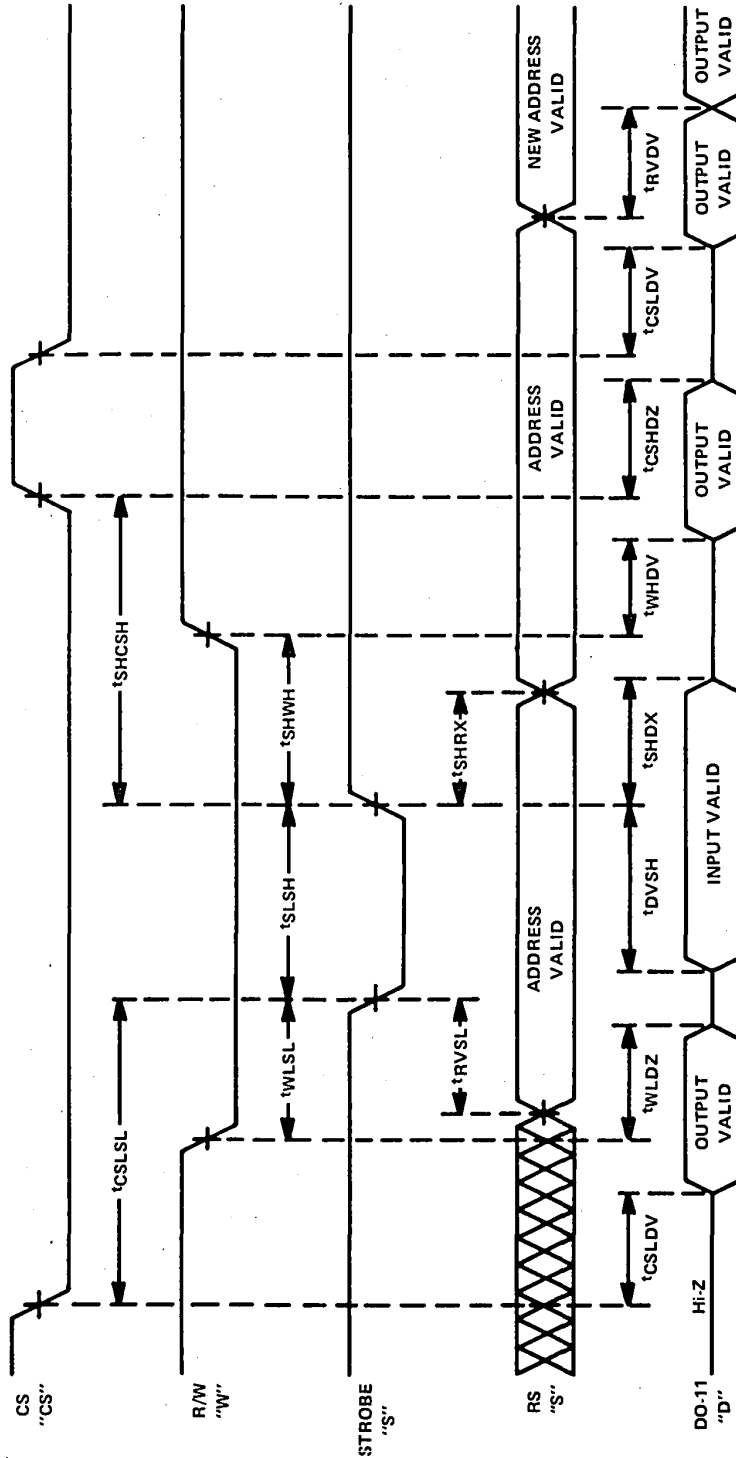


FIGURE 1—WRITE AND READ MODES



TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613  
MEMORY MAPPERS WITH OPEN-COLLECTOR OUTPUTS

TIMING DIAGRAMS

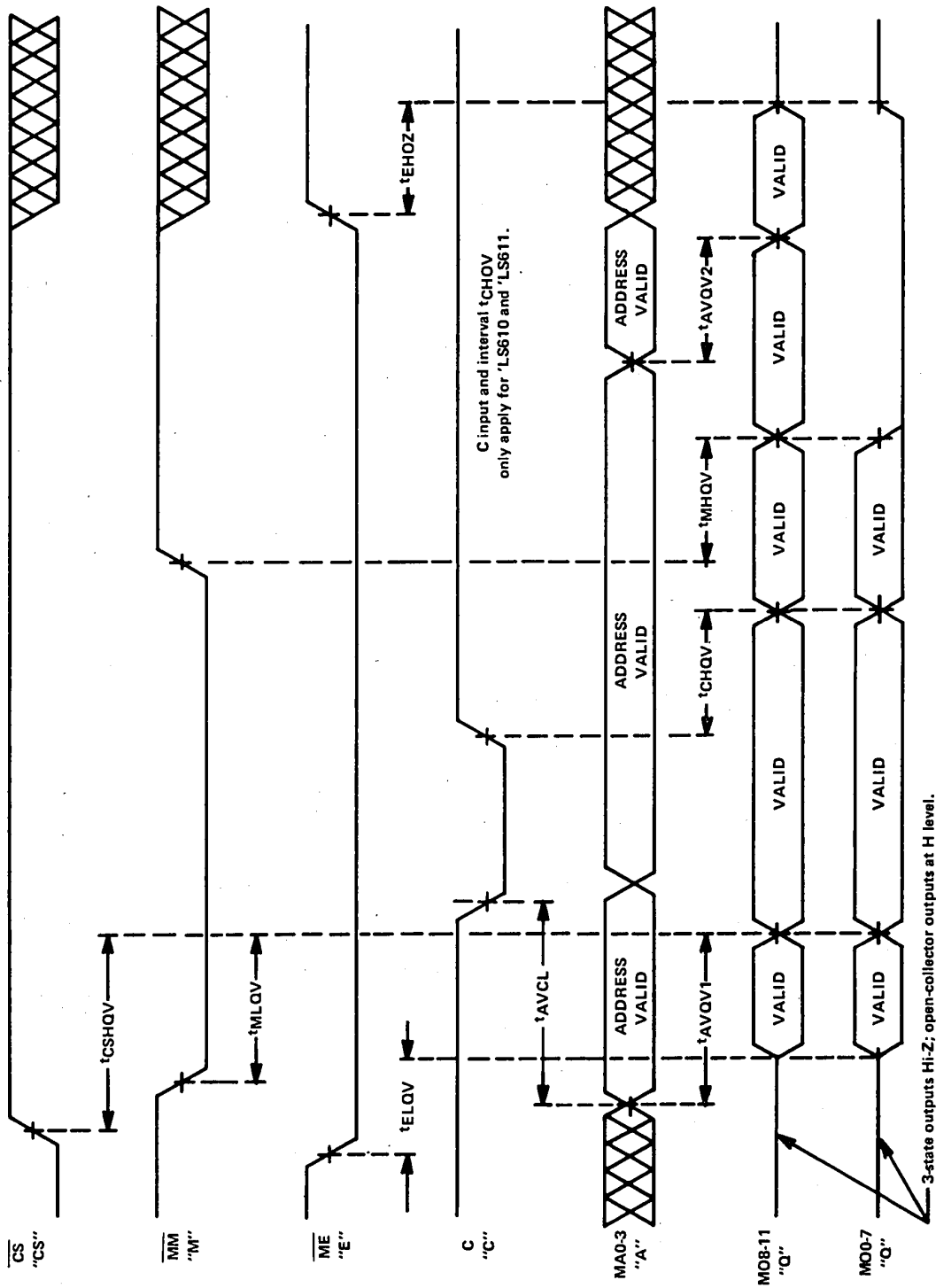


FIGURE 2—MAP AND PASS MODES