DECEMBER 1972—REVISED DECEMBER 1983

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS
for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

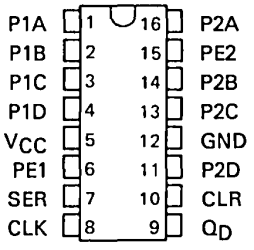
description

These monolithic shift registers which utilize transistor-transistor logic (TTL) circuits in the familiar Series 54/74 configuration, are composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to a low output level by applying a high-level voltage to the clear input while the internal presets are inactive (high). See the preset function table below. Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to either the P1 or P2 inputs of each register stage (A, B, C, and D) with the corresponding preset enable input, PE1 or PE2, high. Presetting, like clearing, is independent of the level of the clock input.

SN5494 . . . J OR W PACKAGE
SN7494 . . . J OR N PACKAGE
(TOP VIEW)



Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be setup at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a low level and the internal presets must be inactive (high) when clocking occurs.

PRESET FUNCTION TABLE
(BIT A, TYPICAL OF ALL)

PRESET INPUTS				INTERNAL
PE1	P1A	PE2	P2A	PRESET A
L	X	L	X	H (inactive)
L	X	X	L	H (inactive)
X	L	L	X	H (inactive)
X	L	X	L	H (inactive)
H	H	X	X	L (active)
X	X	H	H	L (active)

REGISTER FUNCTION TABLE

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	X	X	H	H	H	H
H	H	H	H	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	L	H	L	L	X	H	Q_{B0}	H	Q_{D0}
H	H	H	H	L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	H	H	L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}

H = high level (steady state), L = low level (steady state), X = irrelevant, ↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5494 Circuits . . . . . −55°C to 125°C
SN7494 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

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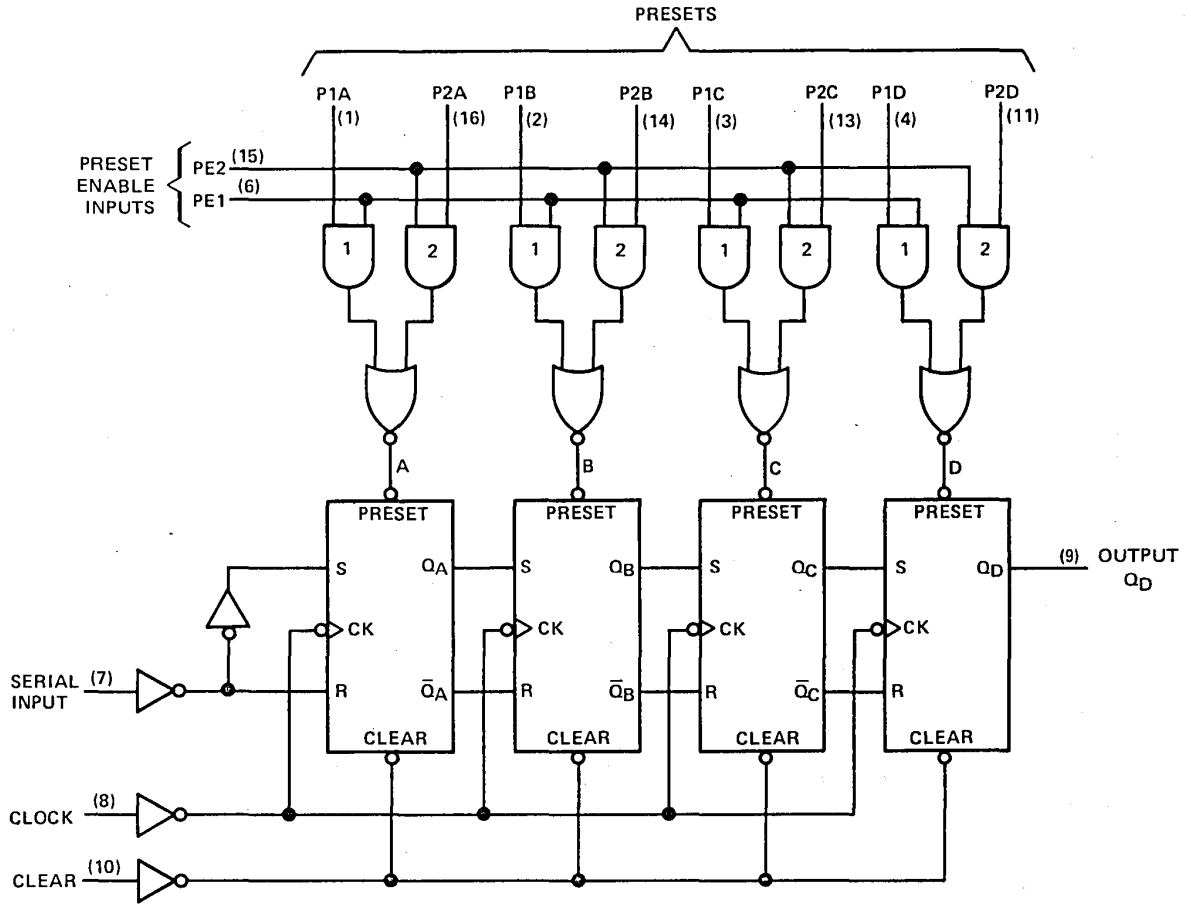
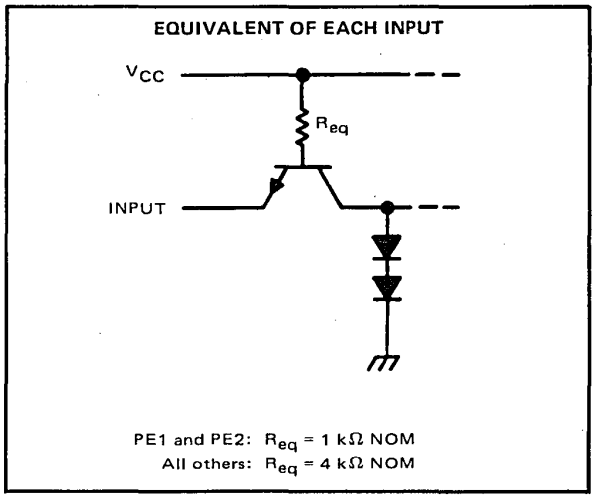
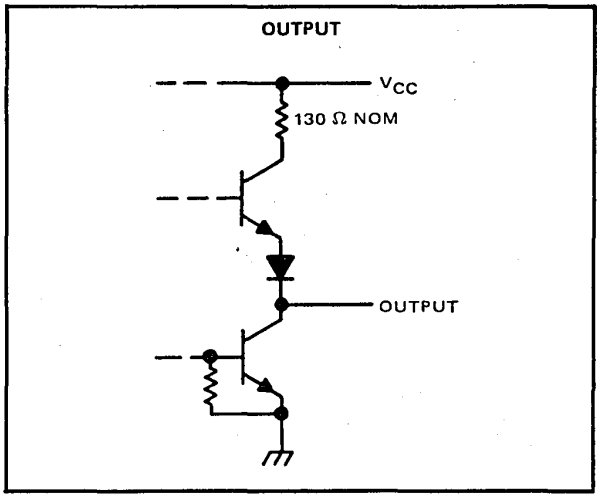
logic diagram



Pin numbers shown on logic notation are for J or N packages.

schematics of inputs and output





recommended operating conditions

		SN5494			SN7494			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, $t_{w(clock)}$		35			35			ns
Width of clear pulse, $t_{w(clear)}$		30			30			ns
Width of preset pulse, $t_{w(preset)}$		30			30			ns
Setup time, t_{su}	High-level data	35			35			ns
	Low-level data	25			25			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5494			SN7494			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 2.4 V			160			160	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 0.4 V			−6.4			−6.4	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		35	50		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the outputs open, clear grounded following momentary application of 4.5 V, both preset-enable inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 4	10			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			25	40	ns
t_{PHL}	Propgaation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset				35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				40	ns

NOTE 4 See General Information Section for load circuits and voltage waveforms.

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