

**Revision History**  
**32K x 8 BIT HIGH SPEED CMOS SRAM**

Revision	Details	Date
Rev 1.0	Initial Release	June. 2024

## FEATURES

- Fast access time :15ns
- Low power consumption:  
 Operating current : 80mA (5V TYP)  
                                   40mA (3V TYP)  
 Standby current : 1mA /0.5mA (5V/3V TYP)
- Wide power supply: 2.7V ~ 5.5V
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- Package : 28-pin 300 mil Skinny PDIP

## GENERAL DESCRIPTION

The AS7C256C is a 262,144-bit high speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

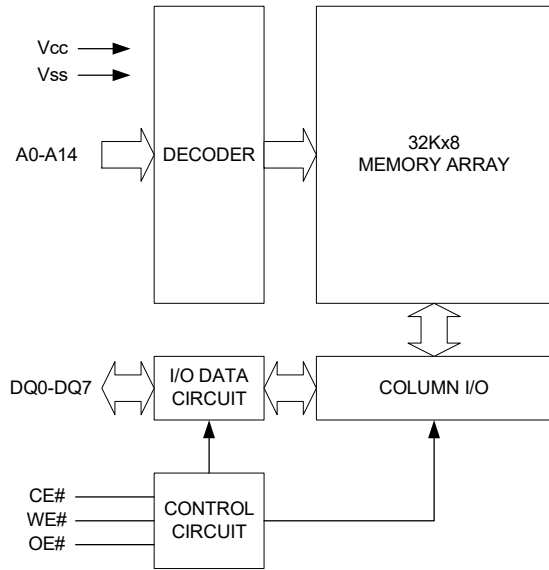
The AS7C256C is well designed for high speed system application. Easy expansion is provided by using an active LOW Chip Enable(CE#). The active LOW Write Enable(WE#) controls both writing and reading of the memory.

The AS7C256C operates from a single power supply. The range of supply voltage is from 2.7V to 5.5V and all inputs and outputs are fully TTL compatible.

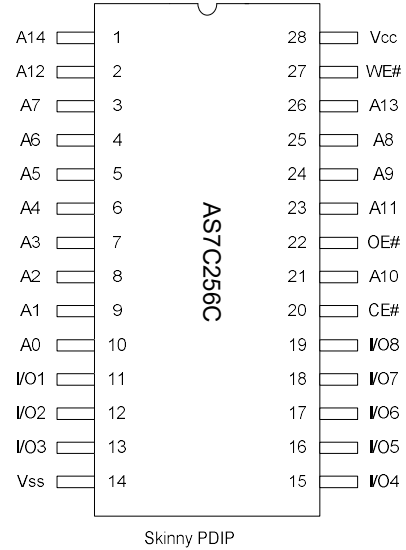
## ORDERING INFORMATION

Product	Operating Temperature	V <sub>CC</sub> Range	Speed	Power Dissipation	
				(I <sub>SB1</sub> ,TYP.) 5V/3V	(I <sub>CC</sub> ,TYP.) 5V(3V)
AS7C256C-15PCN	0 ~ 70°C	2.7 ~ 5.5V	15ns	1mA/0.5mA	80mA (40mA)

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
$V_{cc}$	Power Supply
$V_{ss}$	Ground

## ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on $V_{CC}$ relative to $V_{SS}$	$V_{T1}$	-0.5 to 6.5	V
Voltage on any other pin relative to $V_{SS}$	$V_{T2}$	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	$T_A$	0 to 70	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

## TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	$I_{SB1}$
Output Disable	L	H	H	High-Z	$I_{CC}$
Read	L	L	H	$D_{OUT}$	$I_{CC}$
Write	L	X	L	$D_{IN}$	$I_{CC}$

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.

## DC ELECTRICAL CHARACTERISTICS

For  $V_{CC} = 2.7V \sim 5.5V$

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>*4</sup>	MAX. <sup>*5</sup>	UNIT
Supply Voltage	$V_{CC}$		2.7	5.0	5.5	V
Input High Voltage	$V_{IH}^{*1}$		2.4	-	$V_{CC}+0.5$	V
Input Low Voltage	$V_{IL}^{*2}$		-0.5	-	0.8	V
Input Leakage Current	$I_{LI}$	$V_{CC} \cong V_{IN} \cong V_{SS}$	-1	-	1	$\mu A$
Output Leakage Current	$I_{LO}$	$V_{CC} \cong V_{OUT} \cong V_{SS}$ , Output Disabled	-1	-	1	$\mu A$
Output High Voltage	$V_{OH}$	$I_{OH} = -4mA$	2.4	-	-	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 8mA$	-	-	0.4	V
Average Operating Power supply Current	$I_{CC}$	Cycle time = MIN. CE# = $V_{IL}$ , $I_{I/O} = 0mA$ Others at $V_{IL}$ or $V_{IH}$	-	80	140	mA
Standby Power Supply Current	$I_{SB1}$	CE# $\cong V_{CC} - 0.2V$ , Others at 0.2V or $V_{CC}-0.2V$	-	1	5	mA

For V<sub>CC</sub>= 2.7~3.6V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>*4</sup>	MAX. <sup>*5</sup>	UNIT
Supply Voltage	V <sub>CC</sub>		2.7	3.3	3.6	V
Input High Voltage	V <sub>IH</sub> <sup>*1</sup>		2.0	-	V <sub>CC</sub> +0.5	V
Input Low Voltage	V <sub>IL</sub> <sup>*2</sup>		- 0.5	-	0.6	V
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≧ V <sub>IN</sub> ≧ V <sub>SS</sub>	- 1	-	1	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≧ V <sub>OUT</sub> ≧ V <sub>SS</sub> , Output Disabled	- 1	-	1	μA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	2.4	-	-	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	-	0.4	V
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = MIN. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Others at V <sub>IL</sub> or V <sub>IH</sub>	-	40	50	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≧ V <sub>CC</sub> - 0.2V, Others at 0.2V or V <sub>CC</sub> -0.2V	-	0.5	3	mA

- Notes:
- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
  - V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
  - Over/Undershoot specifications are characterized, not 100% tested.
  - Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
  - Max. Values are guaranteed by Product Characterization, not guaranteed or tested

### CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

### AC TEST CONDITIONS

Input Pulse Levels	0.2V to V <sub>CC</sub> - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF + 1TTL, I <sub>OH</sub> /I <sub>OL</sub> = -4mA/8mA

## AC ELECTRICAL CHARACTERISTICS

### (1) READ CYCLE

PARAMETER	SYM.	AS7C256C-15PCN		UNIT
		MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	15	-	ns
Address Access Time	t <sub>AA</sub>	-	15	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	15	ns
Output Enable Access Time	t <sub>OE</sub>	-	7	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	4	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	7	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	ns

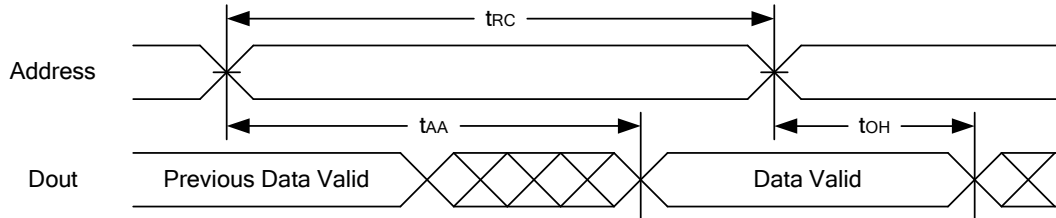
### (2) WRITE CYCLE

PARAMETER	SYM.	AS7C256C-15PCN		UNIT
		MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	15	-	ns
Address Valid to End of Write	t <sub>AW</sub>	12	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	12	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	ns
Write Pulse Width	t <sub>WP</sub>	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	8	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	4	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	8	ns

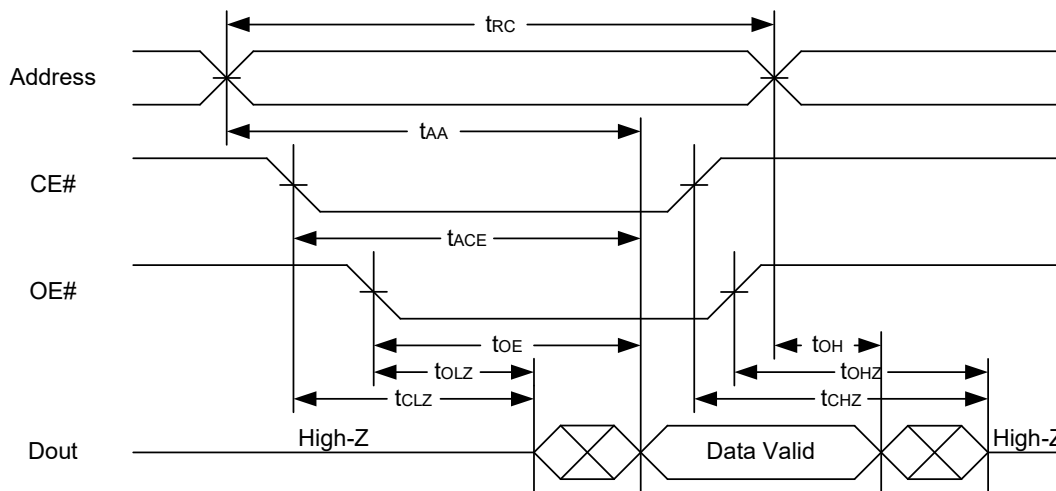
\*These parameters are guaranteed by device characterization, but not production tested.

## TIMING WAVEFORMS

### READ CYCLE 1 (Address Controlled) (1,2)



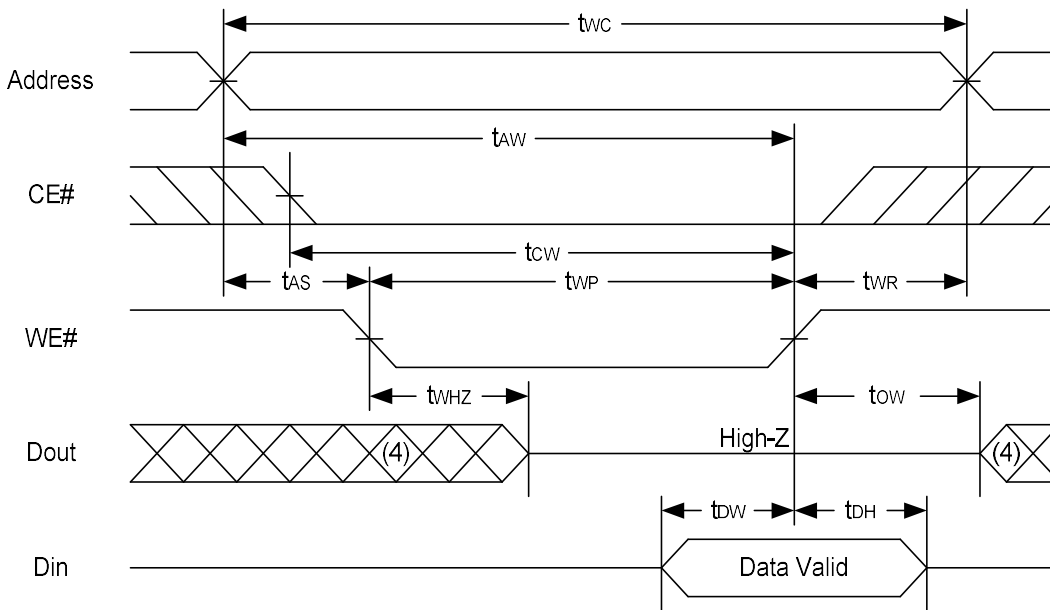
### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



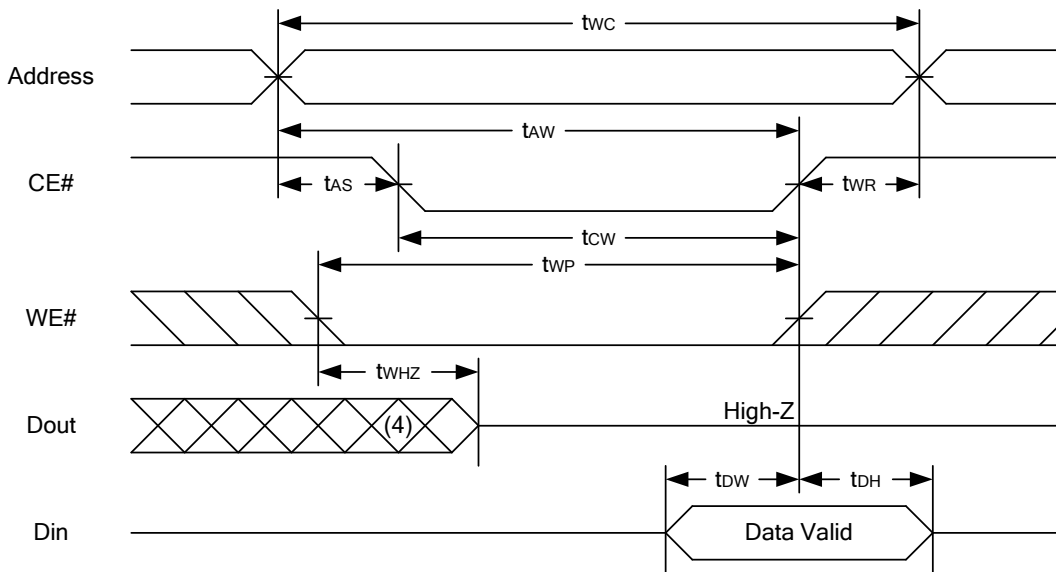
#### Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low.; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

### WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



### WRITE CYCLE 2 (CE# Controlled) (1,4,5)



**Notes :**

1. A write occurs during the overlap of a low CE#, low WE#.
2. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{OW}$  to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

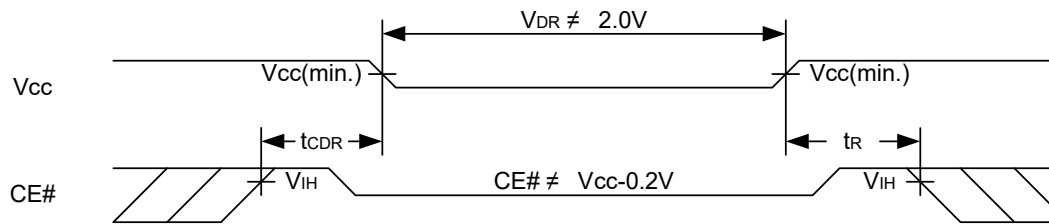


## DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# $\geq$ V <sub>CC</sub> - 0.2V	2.0	-	5.5	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 2.0V, CE# $\geq$ V <sub>CC</sub> - 0.2V	-	0.3	2	mA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC</sub> *	-	-	ns

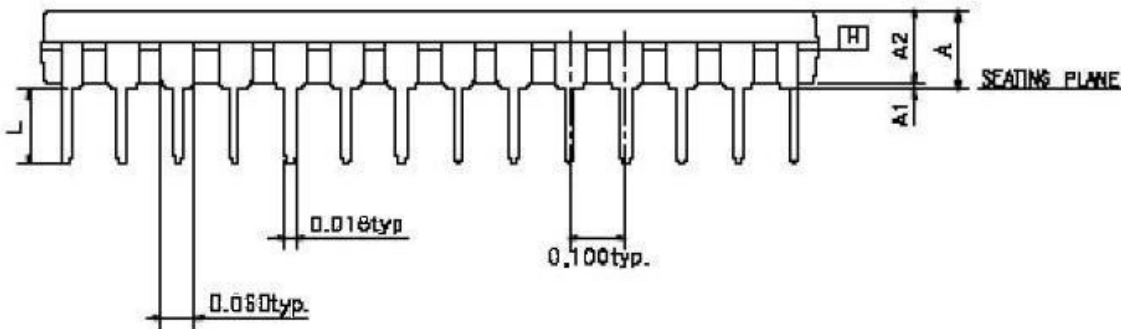
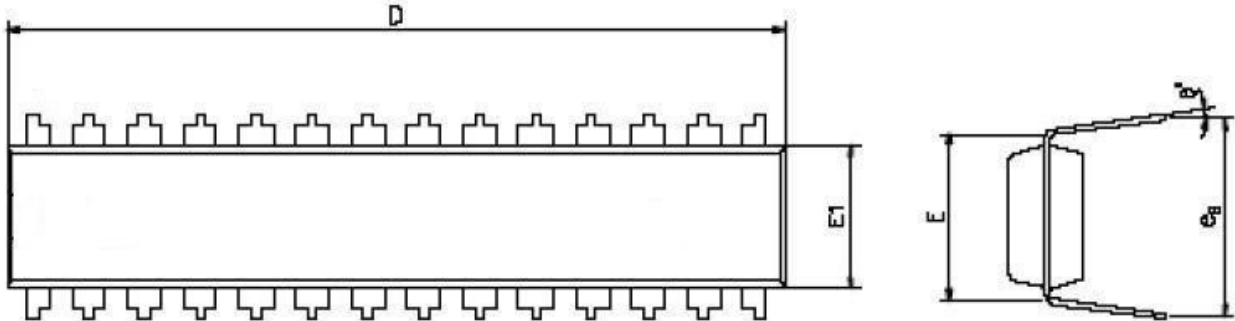
t<sub>RC</sub>\* = Read Cycle Time

## DATA RETENTION WAVEFORM



## PACKAGE OUTLINE DIMENSION

28-pin 300mil PDIP Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
eB	0.330	0.350	0.370
$\theta^\circ$	0	7	15

UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-D15 AH

## Part numbering system

AS7C	256C	-XX	X	X	X	XX
SRAM prefix	Device number 256: 256k (x8) C : revision C	Access time -15 = 15ns	Package: P=DIP 300 mil	Temperature range: C = Commercial 0 ~ 70°C	N=Lead Free and Halogen Free Part	Packing Type None: Tray TR: Reel



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